ESCORT
MODEL 400T

SERVICE MANUAL

Medical Data Electronics • 12720 Wentworth Street • Arleta, California 91331-4329
(800) 237-5243 • (818) 768-6411 • FAX (818) 768-0759

ESCORT Service Manual
Model E400T

ESCORT 400

SERVICE MANUAL

JUNE, 1991

REVISION A

MEDICAL DATA ELECTRONICS
12720 Wentworth Street
Arleta, CA 91331

(818) 768-6411
(800) 237-5243
FAX (818) 768-0759

WARRANTY

ESCORT 400 monitors are warranted against defects in materials and workmanship for the period of 12 months from the date of shipment to original purchaser. Batteries, cables, cuffs and sensors are warranted three months from date of shipment. Warranty is valid only to the original buyer. Defective equipment should be returned freight prepaid. Equipment returned with defective parts and assemblies will be either replaced or repaired. This warranty is not applicable if repair has been attempted or if the instrument has been damaged due to operation outside the environmental and power specifications for the product, or due to improper handling or use.

The foregoing warranty is in lieu of all other warranties expressed or implied, including but not limited to any implied warranty or merchantability, fitness or adequacy for any particular purpose or use. Medical Data Electronics shall not be liable for any special, incidental or consequential damages.

If any default develops, notify Medical Data Electronics, Technical Support Department, giving full details of the difficulty, including the model and serial number of the device. On receipt of the shipping instructions, forward the device prepaid, and repairs will be made at the factory. If requested, an estimate will be made before work begins, provided the device is not covered by warranty.

Factory Service is available by obtaining an RMA number from the MDE Technical Support Department. Please have model number and serial number ready when calling.

WARNING!

To avoid personal injury, the user should not perform any servicing unless qualified to do so.

TABLE OF CONTENTS

PAGE

1.0.0 **ESCORT 400 SPECIFICATIONS** 1-1

2.1.0 **SYSTEM OVERVIEW** 2-1
ESCORT 400 FRONT VIEW 2-2
ESCORT 400 REAR VIEW 2-3
ESCORT 400 INTERCONNECTING DIAGRAM 2-4
ESCORT 400 PLACEMENT BOARD 2-5

3.0.0 **CPU BOARD** 3-1
3.1.0 OVERVIEW 3-1
3.2.0 COMMUNICATION CPU 3-2
3.2.1 Overview 3-2
3.2.2 Clock 3-2
3.2.3 Address Bus 3-2
3.2.4 Data Bus 3-2
3.2.5 Interrupts 3-2
3.2.6 Wait 3-2
3.2.7 Reset 3-3
3.2.8 Read/Write 3-3
3.2.9 Time of Day Clock 3-3
3.2.10 Back-up Battery 3-3
3.2.11 Keyboard 3-3
3.2.12 Tone Generator 3-3
3.3.0 DISPLAY CPU 3-4
3.3.1 Overview 3-4
3.3.2 Clock 3-4
3.3.3 Address Bus 3-4
3.3.4 Data Bus 3-4
3.3.5 Reset and Control Signals 3-4
3.3.6 Interrupts 3-5
3.3.7 Request Lines 3-5
3.3.8 Wait 3-5
3.3.9 Read (lRD*) Write (lWR*) 3-5
3.3.10 Time Tick 3-5
3.3.11 ME/IOE 3-5
3.3.12 Timing 3-6
3.3.13 Video Ram Display Section 3-6
3.3.14 X, Y, Z Axis 3-7
3.3.15 X-Axis Waveform 3-7
3.3.16 Y-Axis Waveform 3-7
3.3.17 Z-Axis Waveform 3-7

CPU WAVEFORM DIAGRAM 3-8

3.4.0 CRT DRIVE CIRCUITRY 3-9
3.4.1 Overview 3-9
3.4.2 Yoke Driver (X-Waveform) 3-9
3.4.3 Yoke Driver (Y-Waveform) 3-9
3.5.0 ANALOG OUTPUTS 3-10
3.5.1 High Level Outputs 3-10
3.6.0 REGULATORS 3-11

CPU BOARD BLOCK DIAGRAM 3-12
CPU SCHEMATICS 3-13
CPU BOARD LAYOUT 3-19
CPU PARTS LIST 3-20

4.0.0 **Z-AXIS BOARD** 4-1

Z-AXIS BLOCK DIAGRAM 4-2
Z-AXIS SCHEMATIC 4-3
Z-AXIS BOARD LAYOUT 4-4
Z-AXIS PARTS LIST 4-5

5.0.0 **DIGITAL SUBCARRIER BOARD** 5-1
5.1.0 OVERVIEW 5-1
5.2.0 MICROPROCESSOR 5-1
5.2.1 Eprom, and Dual Port Ram 5-1
5.2.2 Decoders 5-1
5.2.3 Voltage Regulators 5-2
5.2.4 Amplification of Signal 5-2
5.2.5 Three Channel Filtering 5-2
5.2.6 Switched Capacitor Filters 5-2
5.2.7 Timers 5-3

DIGITAL SUBCARRIER BOARD BLOCK DIAGRAM 5-4
DIGITAL SUBCARRIER BOARD SCHEMATICS 5-5
DIGITAL SUBCARRIER BOARD LAYOUT 5-7
DIGITAL SUBCARRIER BOARD PARTS LIST 5-8

6.0.0 **SWITCHING POWER SUPPLY BOARD** 6-1
6.1.0 INPUT CIRCUITRY 6-1
6.2.0 SYNCHRONIZATION AND SENSE CIRCUITS 6-1
6.3.0 DC OUTPUT VOLTAGES 6-1

SWITCHING POWER SUPPLY BOARD BLOCK DIAGRAM 6-2
SWITCHING POWER SUPPLY BOARD SCHEMATIC 6-3
SWITCHING POWER SUPPLY BOARD LAYOUT 6-4
SWITCHING POWER SUPPLY BOARD PARTS LIST 6-5

7.0.0 **MECHANICAL DISASSEMBLY** 7-1
7.1.0 SAFETY 7-1
7.2.0 FUSE REPLACEMENT 7-1
7.3.0 REASSEMBLY 7-1
7.4.0 DISASSEMBLY 7-1
7.4.1 Top Cover 7-1
7.4.2 Bottom Cover 7-2
7.4.3 Bezel Assembly 7-2
7.4.4 Recorder Removal 7-2
7.4.5 Processor Boards 7-2
7.4.6 Switching Power Supply 7-2
7.4.7 CPU Removal 7-3
7.4.8 CRT Removal 7-3
7.4.9 Z-Axis Board 7-3
7.4.10 High Voltage Power Supply 7-3
7.4.11 Transformer 7-3

CONNECTOR PLACEMENT DIAGRAM 7-4
CHASSIS ASSEMBLY DIAGRAM 7-5
REAR ASSEMBLY DIAGRAM 7-9
LOWER COVER ASSEMBLY DIAGRAM 7-10
MECHANICAL DISASSEMBLY PARTS LISTS 7-11
ANTENNA SYSTEM DESIGN 8-1
ANTENNA SYSTEM SCALE FLOOR PLAN 8-7
ANTENNA SYSTEM SCHEMATIC 8-8
ANTENNA SYSTEM SAMPLE CALCULATIONS 8-9
ANTENNA SYSTEM DESIGN 8-10

SPECIFICATIONS

CHAPTER 1

ESCORT 400 SPECIFICATIONS

DISPLAY

Size: 9" diagonal
Type: CRT non-fade, P31 phosphor
Number of Traces: 4
Trace Length: 4.4 seconds at 25mm/sec

FRONT PANEL KEY FUNCTIONS

Freeze, Record, Alarm Suspend, Record Stop, Page Home, Next Page, Softkeys

CHANNELS

Four Channel

200 MHZ RECEIVER

Input Carrier Range: 174 to 216 MHz
Tunable Range: 42 MHz
Carrier Freq Resolution: 2.5 KHz
IF Frequency: 21.4 MHz
Selectable Channels: Up to 840
Sensitivity: 1 uV typical
Image Rejection: 70 dB
Input Signal Range: -20 to -110 dBm
Modulation Type: FM/FM
Subcarrier Frequency: 800 to 8000 Hz
Signal Outputs: Lead fail, low battery, remote record, pacer, cal

450 MHZ RECEIVER

Input Carrier Range: 457 to 470 MHz
Tunable Range: 13 MHz
Carrier Freq Resolution: 12.5 KHz
IF Frequency: 21.4 MHz
Selectable Channels: 227
Sensitivity: 1 uV typical
Image Rejection: 50 dB
Input Signal Range: -20 to -110 dBm
Modulation Type: FM/FM
Subcarrier Frequency: 1000 Hz
Signal Outputs: Lead fail, low battery, remote record, pacer

ECG

Range: 10 to 300 BPM
Accuracy: ±2% or ±2 BPM
Sweep Speed: 12.5, 25, 50 mm/sec selectable
High Limit Range: 50 to 250 BPM
Low Limit Range: 20 to 150 BPM
Limit Resolution: 5 BPM
Asystole Alarm: R to R interval greater than 6 seconds
Bandwidth: 0.5 to 40 Hz (monitor) 0.05 to 100 Hz (diagnostic)
R-wave Indicator: Flashing heart
Sensitivity: .25 to 3mV/cm selectable (12 levels)
Overload Recovery: 2 sec excluding electrode polarization
Configuration: Neonatal/Adult softkey

RECORDER

Print Method: Thermal array
Channels: Single
Resolution: 8 dots/mm vertical, 32 dots/mm horizontal
Paper: 40 mm grid; 50 mm paper width
Speed: 12.5, 25, 50 mm/sec
Manual Record Duration: 16 seconds
Memory: 12 seconds
Annotation: Channel ID, time, date, all parameter values, scales, source, speed, Bed ID

TRANSMITTER COMPATIBILITY

VHF

ABBOTT TR4
*ACCUCORE (PENDING)
BD ELECTRODYNE TLT2
BURDICK/KONE (PCI)
DATAMEDIX TLT2A
DATASCOPE (PCI)
E FOR M/HONEYWELL TT31, TT32, TT33
GE PDS 3020, 3100
LITTON/DATAMEDIX (PCI)
LSE TM8
*MARCOM
MARQUETTE 9416
MDE ESCORT 1100 (PCI)
MDE ESCORT 1200
MENNEN 419, 219
NIHON KOHDEN 311, 312, 654
*PHYSIO CMS 6000 (MARCOM)
PHYSIO CMS 8000
PPG TT32, TT33
QUINTON 418, 419, 420
SIEMENS 400 (PCI)
SPACELABS 200, 300, 310

UHF

HP78100
*HPM 1400A
MDE ESCORT 1200LR
*SPACELABS 90340

*MUST BE FACTORY CONFIGURED TO WORK EXCLUSIVELY WITH SPECIFIC MODEL

TREND (STANDARD IN 400T)

Parameter: HR
Time: 1, 8, 24 hours

PHYSICAL

Size: 11 (H) x 11 1/4" (W) x 15 3/4" (D)
Weight: 33 lbs.
Environment: 5 to 40 degrees C
0 to 90% humidity
AC Main: 115 VAC ±10%, 60 Hz
220 VAC ±10%, 50 Hz optional
Power: 100 watts

ESCORT TRANSMITTERS (MODEL 1200, 1200LR)

Frequency: 174 to 216 MHz per FCC PART 15 (Model 1200)
462 to 465 MHz per FCC PART 90.217 (Model 1200LR)
Frequency Stability: ±.0025% over operating temp range
Frequency Set: .0015%
Modulation: FM/FM, 2160 Hz subcarrier (Model 1200)
FM/FM, 1000 Hz subcarrier (Model 1200LR)
Deviation: ±3 KHz (Model 1200), ±2.5 KHz (Model 1200LR)
Signal Input Configuration: 3 lead wire
Frequency Response: .5 to 50 Hz (standard)
(Model 1200-01/1200LR-01)
.05 to 100 Hz (diagnostic)
(Model 1200-02/1200LR-02)

Non Linearity: ±1% max
Input Dynamic Range: ±4 mV
Input DC Bias Offset: 100 mV
Common Mode Rejection: 80 dB
Input Impedance: 1 megohm RA to LL (Lead II)
Defibrialltor Protection: 3000V for 10 msec
Power Output: 100 to 150 uV/meter at 100 feet (Model 1200)
5 mW (Model 1200LR)
Antenna: Shielded lead wire set (18 inches)
Battery: 8.4V mercury or 9V alkaline configurable
Battery Life: 7 days (Model 1200)
2.5 days (Model 1200LR)
Activation: By battery insertion
Operating Temperature: 15 to 55 degrees C
Weight: 6 ounces with battery
Size: 1" x 2.38" x 3.75"
Range: 100 feet line of sight (Model 1200)
450 feet line of sight (Model 1200LR)
Cerfification: FCC Part 15 (VHF)
FCC Part 90.217 (UHF)
UL 544 (Model 400T)

SYSTEM OVERVIEW

CHAPTER 2

2.0.0 E400T SYSTEM OVERVIEW

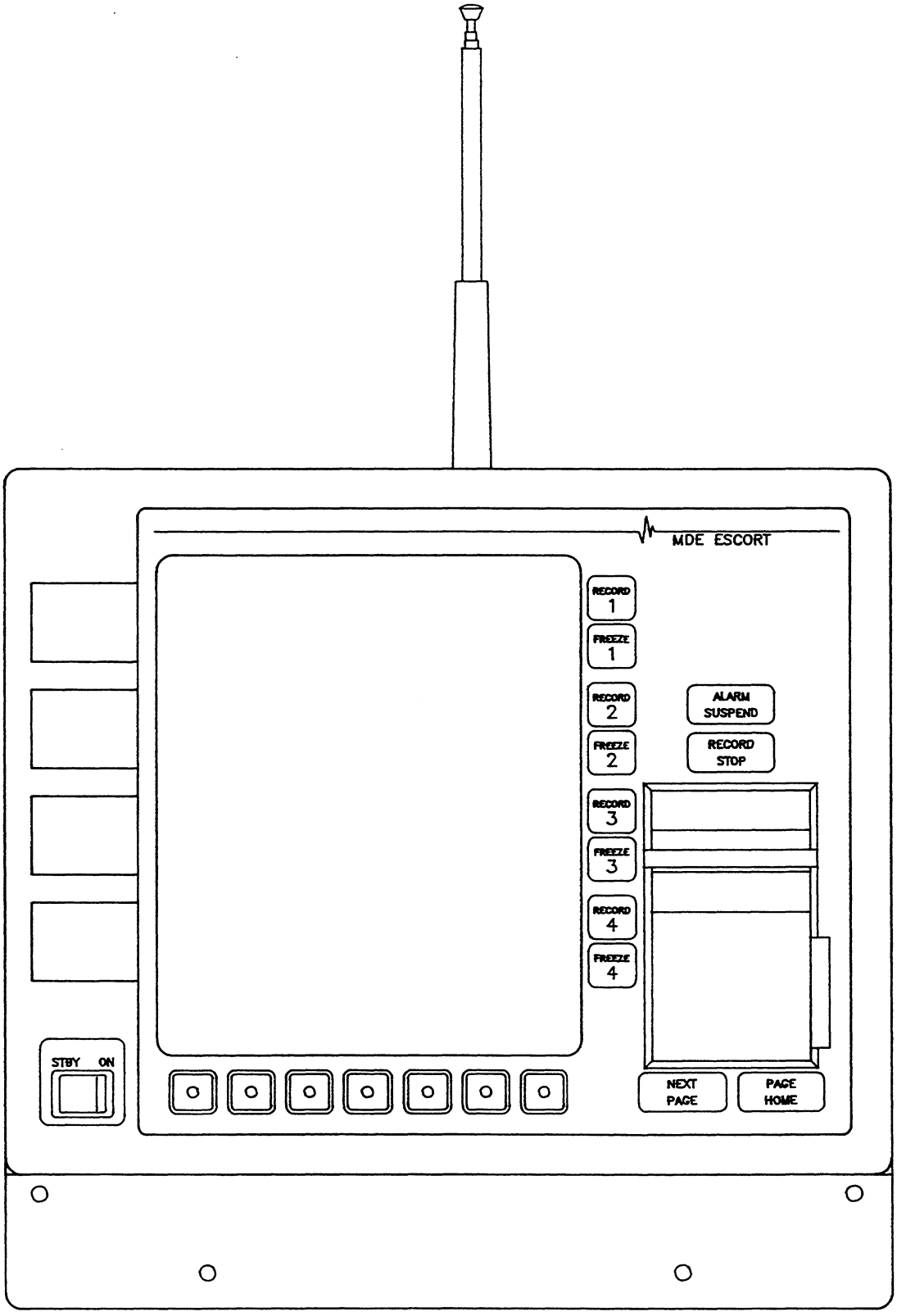
The **ESCORT 400T** is a four patient telemetry monitor. It is factory configurable for either 200 MHz or 450 MHz operation. If configured for 200 MHz it is programmable for most transmitter brands, including all their TV bands and channels within that FCC allowable frequency range. If configured for 450 MHz, it is programmable for Hewlett Packard and Medical Data Electronics Long Range Transmitters.

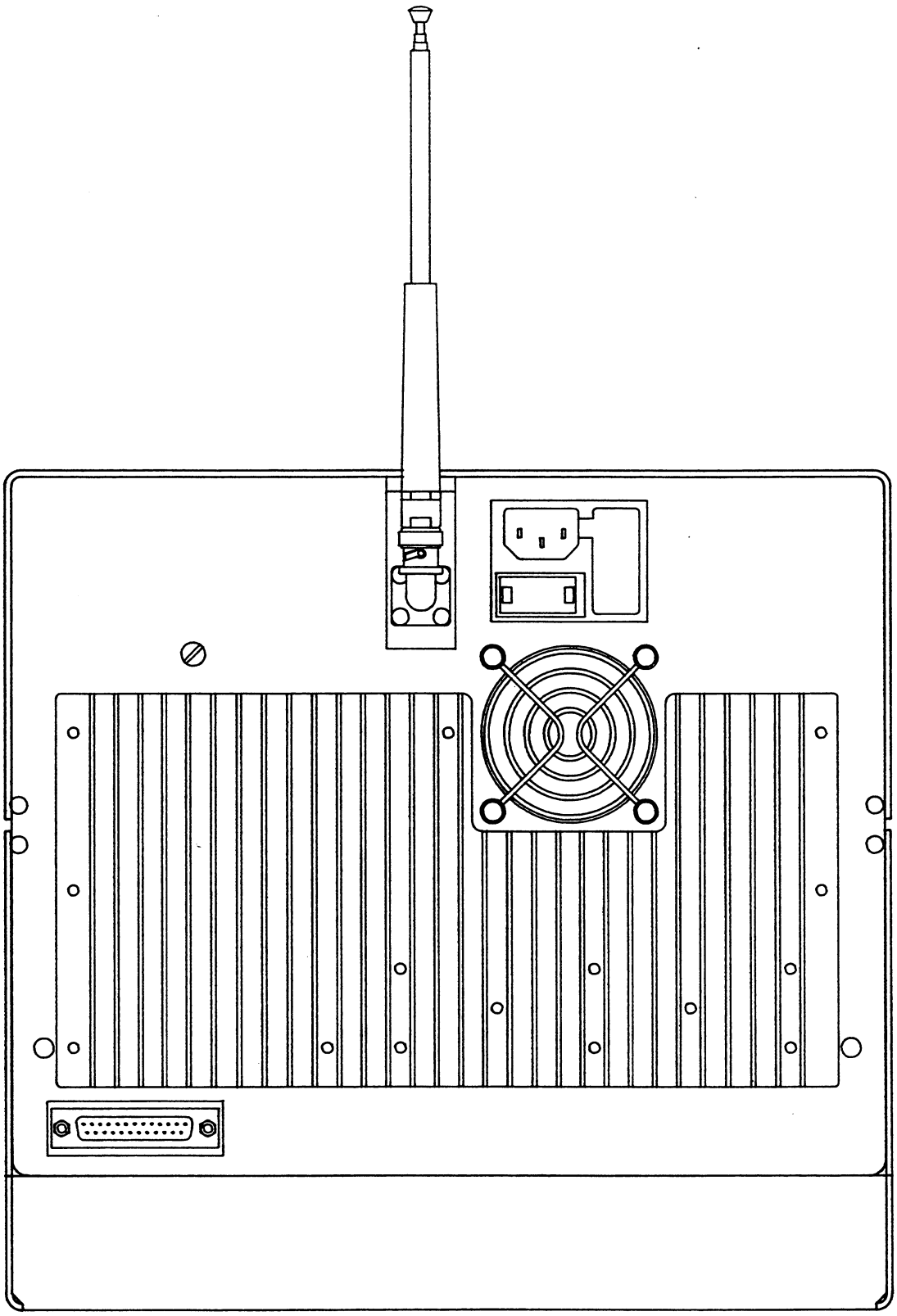
The **400T** receives an FM/FM modulated signal through the antenna which passes the signal to an active splitter. The splitter directs the signal to four separate receivers, channels 1-4. The receivers strip off the first FM carrier and sends the subcarrier signal on to the digital subcarrier boards. The digital subcarriers will further demodulate, filter, and digitize the ECG signal to send to the CPU Board for processing and display on the CRT.

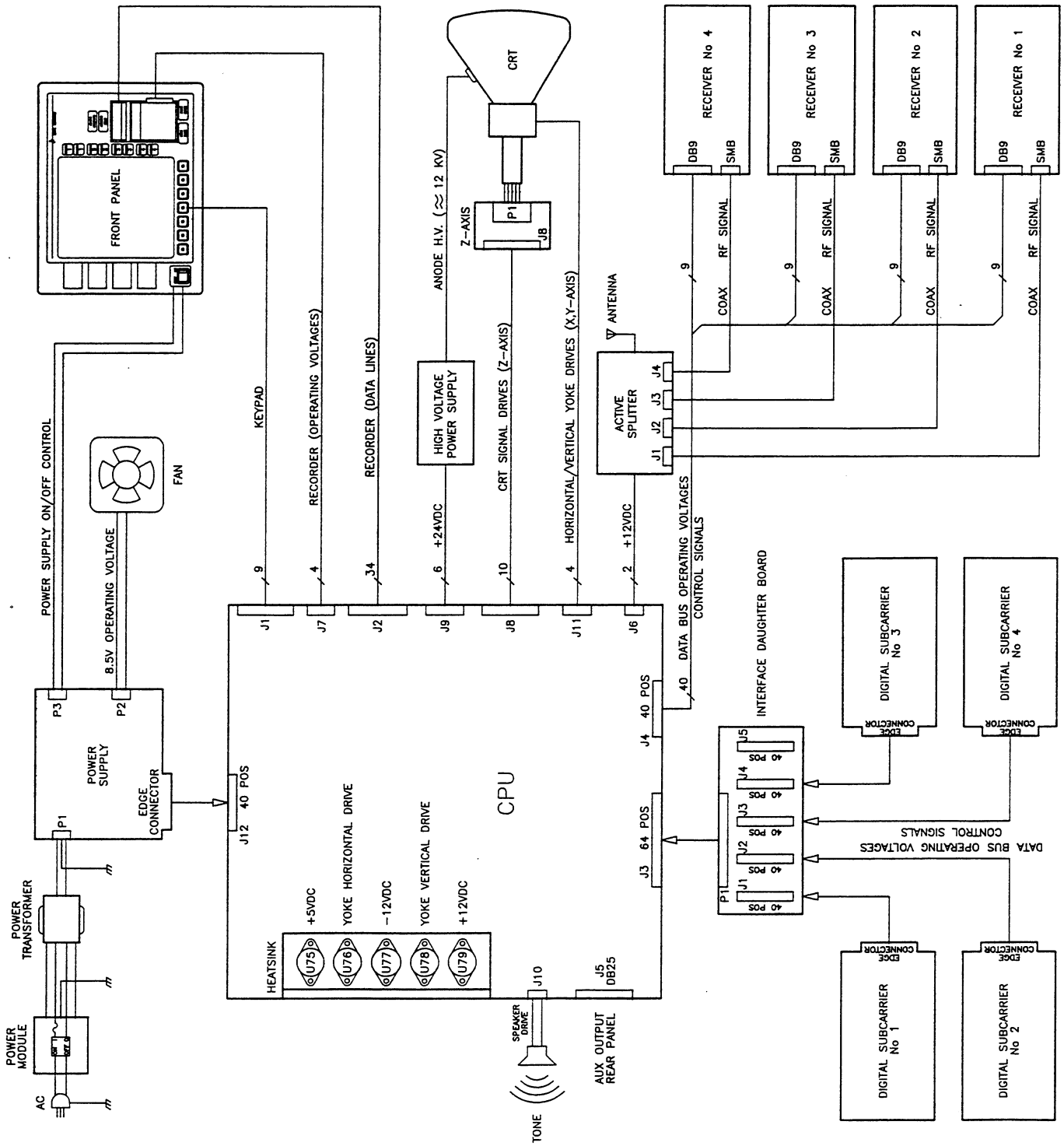
The CPU Board handles various processing tasks for the monitor as well as interfacing to the CRT display and recorder. High level outputs are available at the auxiliary connector on the rear panel. This information can include waveform information, and alarm status; these outputs are programmable in the configuration pages.

The digital subcarrier board digitizes the ECG from the subcarrier signal. It also decodes for subtones which can be lead fail, low battery, cal pulse, or remote record indicators from the transmitter. The waveform, cardiotach, pacer and subtone information is relayed to the CPU Board through a dual port RAM.

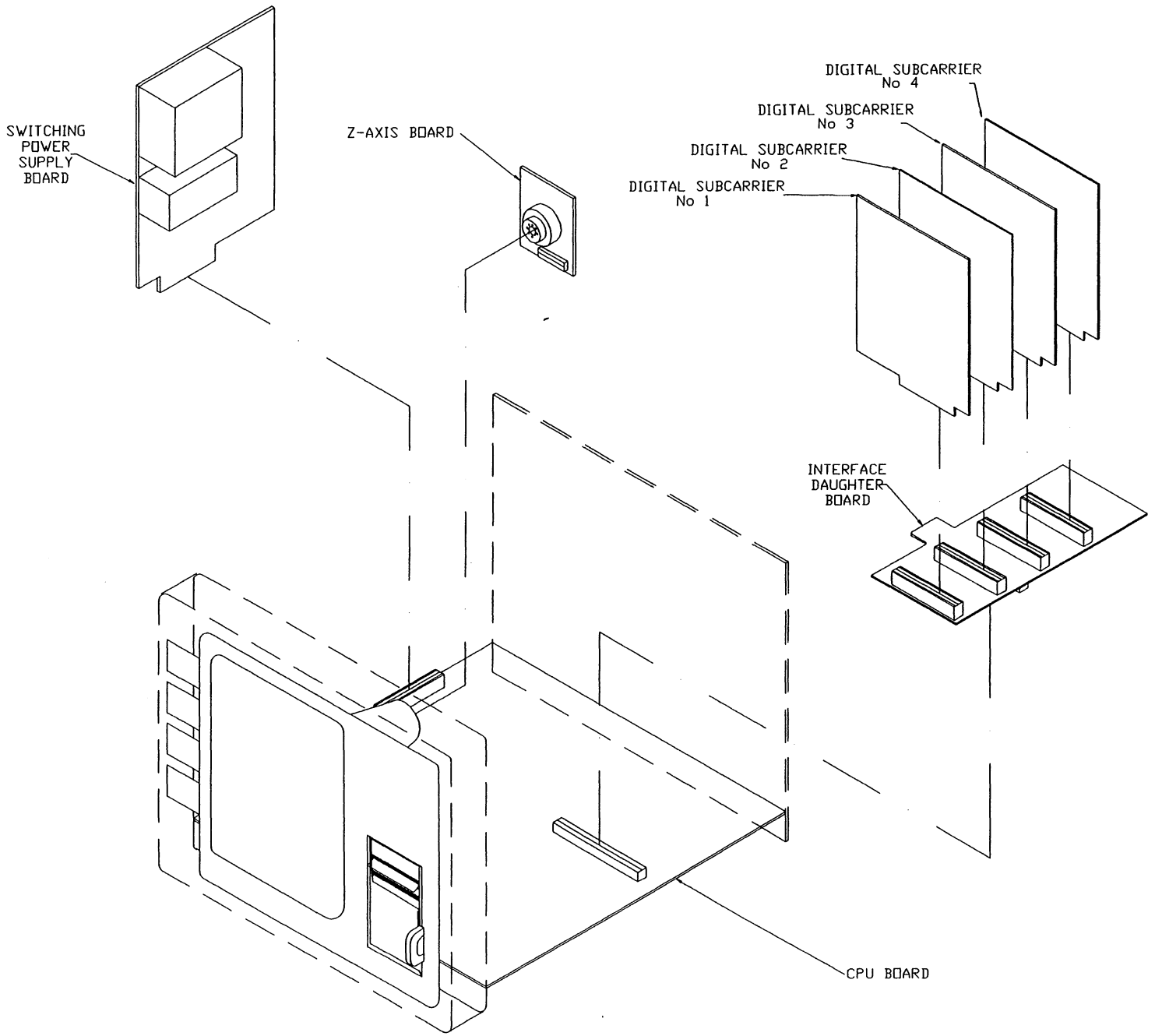
The Switching Power Supply Board provides operating voltages of +48V, +25V, +15V, -15V, and +8.5V. These voltages go to the CPU board and are used throughout the monitor.


MDE ESCORT
RECORD 1
FREEZE 1
RECORD 2
FREEZE 2
RECORD 3
FREEZE 3
RECORD 4
FREEZE 4
ALARM SUSPEND
RECORD STOP
STBY ON
NEXT PAGE
PAGE HOME





ESCORT IV INTERCONNECTION DIAGRAM



400T BOARD PLACEMENT

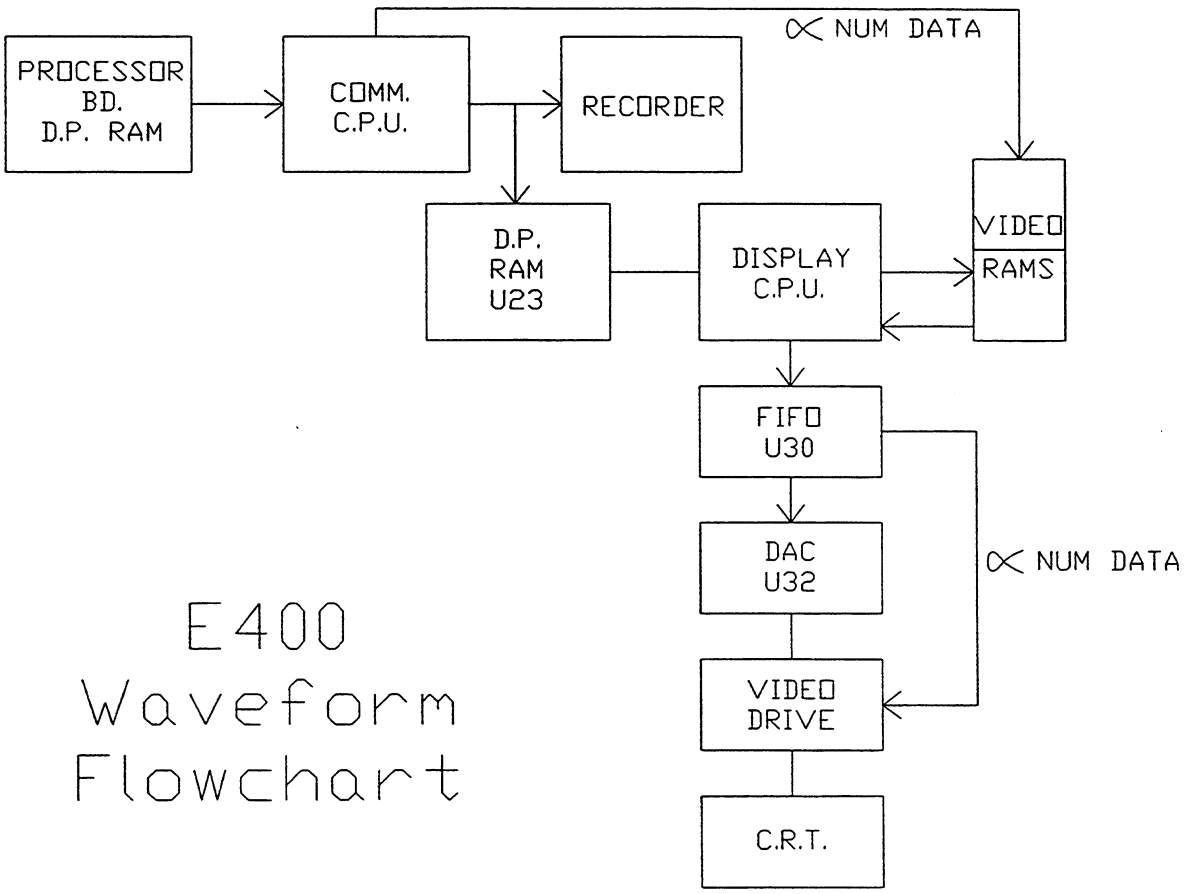
CPU BOARD

CHAPTER 3

3.0.0 CPU BOARD

3.1.0 THEORY OF OPERATION OVERVIEW

The CPU Board uses two Z80 based 64180 microprocessors. Each has its own set of tasks to perform which is independent from the other. The tasks that each performs is determined by their respective EPROM's. The first microprocessor, the display CPU, controls tasks needed to drive and display information on the CRT. The second microprocessor, the communication CPU, manages data transferring from the four processor cards such as, ECG data, storing that information temporarily into memory and notifying the display CPU that waveform data is available. Using the flow chart below, one can see the process of obtaining the waveform information and transferring it onto the screen. The two microprocessors have its own 18 bit address and 8 bit data bus, each with its own set of supporting hardware which enable them to function independently. They exchange timing data through the video RAM display section. The CRT drive section provides the necessary amplification and biasing needed to drive the CRT.



E400 Waveform Flowchart

3.2.0 COMMUNICATION CPU

3.2.1 OVERVIEW

The communication microprocessor and its supporting circuitry has the task of communicating and transferring data to and from the four processor cards. This information is stored in the dual port RAM (U23), to be used by the display CPU section as needed.

3.2.2 CLOCK

The clock for the communication microprocessor is the same 16 MHz crystal, X-1 used for the display microprocessor.

3.2.3 ADDRESS BUS

There is an 18 bit address bus (pins 13-30) that governs communication to all devices relating to the communication CPU. This includes, the 64K X 8 EPROM (U13), and two 32K X 8 static RAMS (U18, U24). Addresses 2A0-2A12 are used for two 8K X 8 video RAMS (U52 and U51) and the 2K X 8 dual Port RAM (U23). Addresses 2A14-2A17 manage the dual 2-4 line decoder/demultiplexer. U25, a 3-8 line decoder/demultiplexer use addresses 2A11-2A13, while 2A0-2A3 are used for the real time clock (U28). 2A0-2A11 of the address bus are also routed to the 64 Pin connector (J3) for communication with the four processor cards.

3.2.4 DATA BUS

The 8 bit data bus 2D0-2D7 (Pins 34-41) are used for all memory devices (U13, U18, U24, U51, U52 and U23). These are also used for the D to A tone generator (U26), an inverting octal buffer, U20, and the real time clock, (U28). The data bus interfaces with the recorder and the processor cards through J2 and J3 respectively.

3.2.5 INTERRUPTS

TIME TIC* is an input to interrupt 1 at pin 10 of the communication microprocessor. TIME TIC* is a synchronization signal for communication between the microprocessor and the four processor cards. Interrupt 2, pin 11, is the record (BUSY*) signal from the recorder.

3.2.6 WAIT

The 2 BUSY* signal is an input to the wait line (pin 4). This busy signal is an output from U23 pin 45 that tells the communication microprocessor that the memory location it attempted to access in U23 was already being addressed by the display microprocessor, thus delaying its request.

3.2.7 RESET

The communication microprocessor uses the same power-on clear circuit that the display microprocessor does, the only difference being that the RESET OUT* signal for the communication microprocessor is isolated from the display reset signal through an OR gate.

3.2.8 READ/WRITE

The READ (2 RD*) and WRITE (2 WR*) signals are outputs from the communication microprocessor at pins 63 and 62 respectively. The READ signal is used to retrieve data from the four processor cards, and the write signal initiates the downloading of data into the same devices. They also access all memory and I/O devices related to the communication bus.

3.2.9 TIME OF DAY CLOCK

U28 is a real-time clock that has a built in Quartz oscillator, time and date function and CMOS circuitry for low power consumption. The time and date is displayed on the test page and annotated on the recorder strip.

3.2.10 BACK-UP BATTERY

U31 monitors the 5 volt operating voltage for U24 and U28. If +5 volts drops below a critical level, U31 will disable RAM select lines and switch to the 2.4V backup battery. This enables system configuration and, time and date information to be held current.

3.2.11 KEYBOARD

The keyboard encoder has a matrix of four columns (X) and five rows (Y). The columns are scanned at a rate set by C2 and C3. With a key depression, the appropriate X and Y input will go low, disabling the counter. Internal and external circuitry (C1) will debounce the key and locks out any other Y-inputs. Once the debounce circuit times out, the data is latched and the data available signal, pin 13, goes high. This notifies the microprocessor through the programmable I/O device at pin 13. The microprocessor will then activate the encoder's output (pin 14) and read the keypad data through D0-D4.

3.2.12 TONE GENERATOR

U26 is an SAA1099 stereo music synthesizer. Using chip enable (CE*), write enable (WR*), and the address control (A0) signal, data is downloaded into internal registers through the data bus, 2D0-2D7. This data is fed to frequency generators which output an audio tone to pin 4 (OUTR). This audio signal is then conditioned by a bandpass filter, C23, C25, C46, R33, R38 and is amplified by U50. D18 and D19 suppress noise from the signal before it is routed to the speaker at connector J10.

3.3.0 DISPLAY CPU

3.3.1 OVERVIEW

The Display CPU and its supporting circuitry has the task of controlling synchronization of information displayed on the screen and generating vital signals to control the hardware used to drive the CRT.

3.3.2 CLOCK

The clock is a 16 MHz crystal oscillator (X-1) at pin 3 of the display microprocessor, U12.

3.3.3 ADDRESS BUS

There is an 18 bit address bus 1A0-1A18, U12 pins 13-30 that governs communication to all devices relating to the display CPU address bus. These include the 64K X 8 EPROM (U11), and a 32K X 8 static RAM (U17). Addresses 1A0-1A12 are used for two 8K X 8 video RAMS (U52 and U51) and the 2K X 8 dual port RAM (U23). Addresses A0 and A1 are used for the programmable input/output device (U27), while addresses 1A13-1A15 go to the dual 2-4 line decoder/demultiplexer (U8) and the 3 to 8 line decoder/demultiplexer (U10).

3.3.4 DATA BUS

The display microprocessor has an 8 bit data bus 1D0-1D7 that carries data to and from all memory devices (U11, U17, U52 and U51, U23) and the programmable input/output device (U27). 1D0-1D4 are used for the 9 bit parallel to serial encoder (U2).

3.3.5 RESET AND CONTROL SIGNALS

There are three ways the display microprocessor can be reset: 1) Power Down Detect - U1 monitors the 5V reference at pin 2. If this reference drops below a threshold of 4.6V the output of U1 will go low (0V), causing a reset. 2) Hardstart - U4 Pins 1-3, R8, R9, R7, C5 form a hardstart circuit. On power up it keeps the microprocessor in a reset condition until C5 charges up enabling operating voltages to reach their proper levels before the microprocessor starts running. 3) Reset Timer - The third way a reset can be triggered is by the DM reset signal which is generated by the reset timer (U15). If the horizontal sweep 1 signal (HSWP1) is not detected in .79 seconds the output of U15 will become active (high), thus activating the DM RST signal (LOW).

3.3.6 INTERRUPTS

The 64180 display microprocessor has four interrupt pins. This type of configuration only uses one of them, while the others are kept inactive. The interrupt to the processor is horizontal end (HORZ END*), pin 10. HORZ END* goes low when one trace worth of data has been transferred to U30 and tells the microprocessor to adjust its Horz. sweep 1 and 2 signals for the next trace of data.

3.3.7 REQUEST LINES

Direct request 0 (DREQ0*) and direct request 1 (DREQ1*) are used to detect a direct memory access request (DMA REQ*) from the FIFO U30.

3.3.8 WAIT

The 1 BUSY* signal (U23 pin 3) is input to the wait line at Pin 4 of the display microprocessor. It alerts the microprocessor that the memory location it attempted to access in U23 was already being addressed by the communication microprocessor thus delaying its request.

3.3.9 READ (lRD*) WRITE (lWR*)

The READ (lRD*) and WRITE (lWR*) signals are active low outputs from the display microprocessor at pins 63 and 62 respectively. The read signal is used to retrieve data from its associated memory IC's and the PPI (U27). It is also gated with pin 13 of U10 to create the output enable (OE*) for the keypad encoder (U2). The write signal initiates the microprocessor to write data to the CPU RAM, video RAM, and PPI. It is also gated at U16 with pin 10 of U10 to create the write clock for FIFO U30.

3.3.10 TIME TICK

Using a one shot timer (U6) and the T-OUT signal (pin 31) from the display microprocessor as a trigger source, a pulse waveform at the output of U6 (Pin 7) with a duty cycle of 240 uS is generated. This signal is routed to the communication microprocessor (U14) pin 10 and to the processor boards at J3 to synchronize communication between the communication CPU and the four processor cards

3.3.11 ME/IOE

These two signals are utilized for the purpose of distinguishing whether a memory I.C. or I/O device are being addressed.

3.3.12 TIMING

U5, a divide by four counter, takes the 16 MHz clock input at pin 1 and divides it down to 4 MHz at pin 4. This output is fed to the clock input of U7, pin 2, where it is divided by 16 for an output of 250 KHz at pin 15. This signal, CPU TIME, is used to disable DMA requests at U55, pin 6 in order to allow the display CPU to perform internal "Housekeeping" duties. The power supply sync signal (P.S. SYNC) is also generated here, but is isolated through R13, it locks the switching power supply board at an operating frequency of 250 KHz.

U7 has four other outputs. The signal C3 is used for the clock input of the baud rate counter (U47). C4 and C5 are not used. C6 is used at U49, the read clock for FIFO U30, and as the clock input for the next counter U9 which further divides the input to generate a 8/16 clock. This signal is fed to U53, Pin 2, which will be used with U62 to set the position of the alphanumeric data on the screen. 8/16 will also determine the clock frequency for serial transmission of U30. The 8/16 signal is further divided by U5 for an output at Pin 12. This is used as the clock input for the reset timer, U15.

3.3.13 VIDEO RAM DISPLAY SECTION

U51, U52, and U23 and its supporting circuitry control communication between the display and communication microprocessor. They coordinate microprocessor communication between video RAM 1 andvideo RAM 2.

Communication between the microprocessors is accomplished through U23, a dual port RAM. Each microprocessor uses its own READ, WRITE, and chip enable, (1EDPR or 2EDPR) to access any memory location in U23. 1BUSY* and 2BUSY* are activated to let the microprocessors know that the memory location it tried to access is already being addressed by the other, thus delaying its memory access request.

Communication to the video RAMS are controlled by video RAM bank switches U34 through U45, and the bank select signal (BANK SEL). If the bank select signal (pin 9 of each switch) is low (0V) then the top four input signals to the switch (display CPU), pin 2, 6, 11, 15 will be passed through to the video RAM. If the BANK SEL signal is high (5V) then the lower four inputs (communication CPU), pins 1, 3, 10, 12 will be selected. Both video RAM's cannot be accessed simultaneously by the same microprocessor. U46 is used to invert the bank SEL signal so that if, for example, the display CPU is communicating with video RAM 1, the communication CPU will then be communicating with video RAM 0.

3.3.14 X, Y, Z AXIS

When the display CPU is ready to download screen information, FIFO WR* is active at U30, pin 31. Waveform and alphanumerics data (1D0- 1D7) is then downloaded into the 2K memory of U30, a parallel/serial FIFO. When the last WRITE cycle of DMA is completed, the TEND* signal is active. It is shifted out pin 15 to generate the Horizontal End signal (HORZ END*) which tells the display CPU to adjust its Horizontal sweep signals 1 and 2 (HSWP1, HSWP2) for the next trace of data. Waveform data is shifted from the FIFO in parallel mode (Q0-Q7), alphanumeric data is shifted in serial mode at pin 1 (SO). What mode the FIFO shifts out in is determined at pin 38 (SO/PO). Pin 40 is the clock that determines the "Baud Rate" of data in the serial mode. C6, when selected by U49 is the clock for reading data from U30 in parallel or serial mode.

3.3.15 X-AXIS WAVEFORM

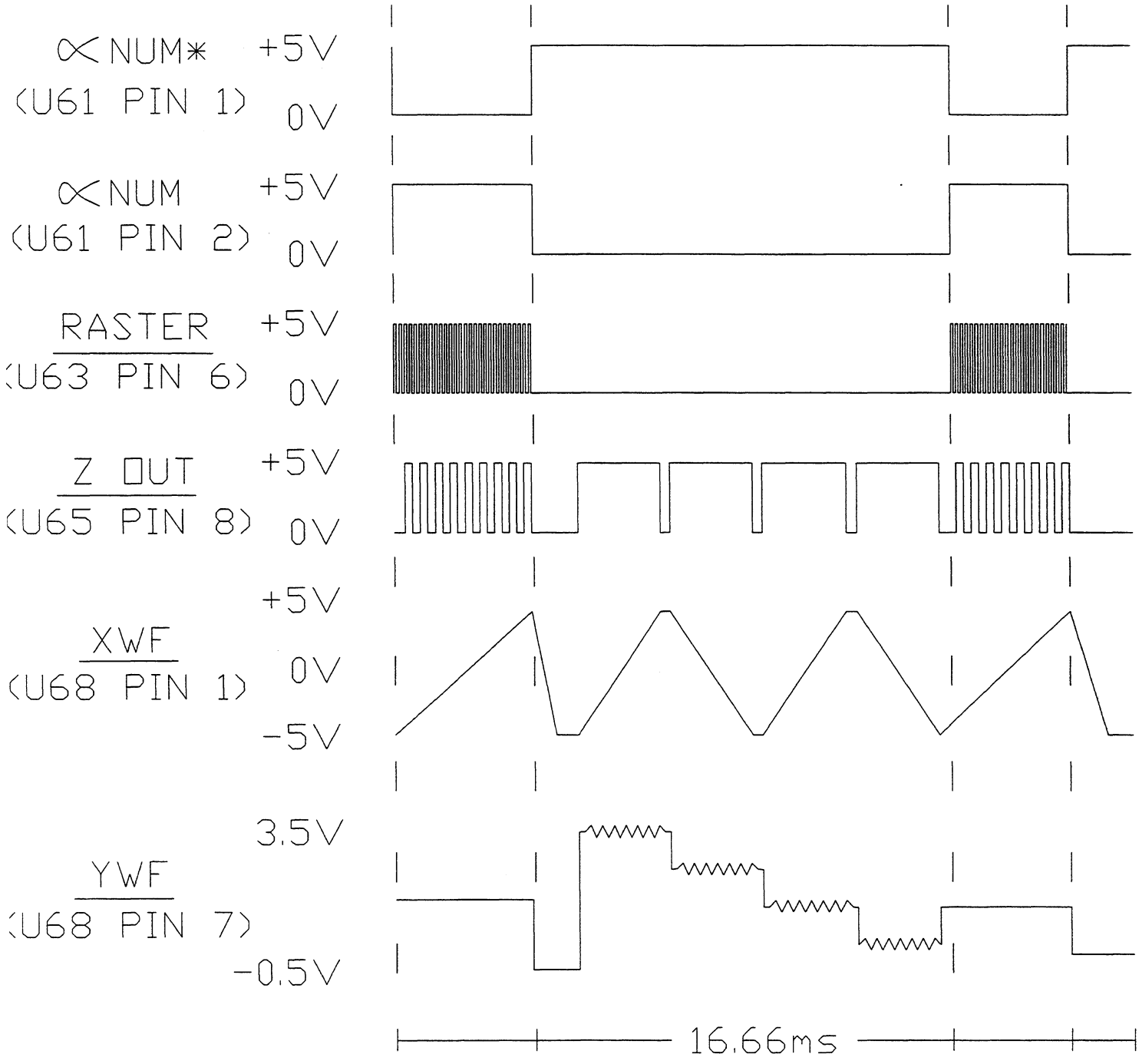
The Horizontal sweep signals (HSWP1, HSWP2) control the slope and polarity of the X-waveform through U67. U67 is a demultiplexer which, depending on inputs A and B will select one of the four reference voltages (Y0-Y3). The selected voltage will then be sent to the integrator circuit through pin 3 of U67. This integrated signal, U68, pin 1, forms the X-axis waveform (see next page). The X-waveform is comprised of five time periods. The first four periods are designated for the waveform mode, the fifth period for the alphanumeric mode. U71 and its supporting circuitry are used to set and adjust the left side blanking (R58) and the right side blanking (R51).

3.3.16 Y-AXIS WAVEFORM

Waveform data is downloaded from FIFO U30 through buffer U33 to the digital to analog converter U32. The analog output is amplified by U68 to form the Y-waveform. The Y-axis waveform contains all ECG data for the four waveform traces. The position of the waveforms on the screen are adjusted by R54, the waveform size is adjusted by R41.

3.3.17 Z-AXIS WAVEFORM

Alphanumeric data is shifted from pin 1 of the FIFO, U30 which when timed with the proper logic signals will create the Z-OUT signal. This signal is routed to the Z-axis board at J8, which will be used as the control voltage for the cathode of the CRT.


∝NUM*
(U61 PIN 1)
+5V
0V
∝NUM
(U61 PIN 2)
+5V
0V
RASTER
(U63 PIN 6)
+5V
0V
Z OUT
(U65 PIN 8)
+5V
0V
XWF
(U68 PIN 1)
+5V
0V
-5V
YWF
(U68 PIN 7)
3.5V
-0.5V
16.66ms

3.4.0 CRT DRIVE CIRCUITRY

3.4.1 OVERVIEW

The power drive circuitry has the task of driving the yoke (X, Y) in order to deflect the CRT electron beam in the proper coordinates. The X-yoke is driven in a continuous mode. The Y-yoke is driven in two modes: 1) A continuous drive and 2) A pulse drive. Waveform video is accomplished in the continuous drive (vector) mode, while alphanumeric video is done in the pulse drive (raster) mode. The high voltage power supply and the Z-axis board provide the proper biasing of the CRT.

3.4.2 YOKE DRIVER (X-WAVEFORM)

X-waveform (XWF) is first amplified by a summing amplifier, U74 pins 5, 6, 7 and supporting circuitry. This is done so that the Horizontal gain (R81) of the screen video can be adjusted and the Horizontal position (R75) can also be adjusted. The X waveform is amplified further by U76 before going to the X yoke at J11. U74, pins 12, 13, 14, and Q3 form a protection circuit. If the system is not functioning properly, the X enable signal will become inactive (HIGH) and disable the X-waveform from driving the yoke. This prevents damage to the system.

3.4.3 YOKE DRIVER (Y-WAVEFORM)

The first stage of signal processing for the Y-waveform is also a summing amplifier. R120 adjusts the four waveforms vertical position and R80 adjusts the vertical gain of the four waveforms. This summed signal is fed through an analog switch, pin 6 to pin 7 of U80 before reaching the last stage of amplification at U78. The amplified Y waveform is used to drive the Y yoke at J11. This continuous (vector) drive method is used to display high quality waveforms on the CRT.

During the alphanumeric (raster) mode, αnum becomes active (high) enabling analog switch U80-A. This allows the alpha numerics vertical size reference voltage to drive the Y yoke. The alpha numerics vertical size can then be adjusted by R72. The αnum signal will simultaneously enable switch U80-D, which will adjust the gain of the Y yoke power amp (U78). Q8 is also biased by the αnum signal which will switch Q4 on, thus boosting the power amplifier (U78) supply voltage to 48V.

The αnum* signal is active (LOW) in sync with the αnum signal. It will disable the Y waveform (trace data) from reaching the power amp (U78) during the alphanumeric (raster) mode at analog switch U80- B. This signal will also disable switch U80-C, which, with R135, R107 and R101 adjusts the gain of U78 during the waveform mode. R135 adjusts the frequency response of the four waveform traces.

While both anum signals are active, the RASTER signal becomes active generating a 41.6 KHz square wave. This square wave is inverted and the logic level is raised to 12 volts (high) by Q4 and Q5 and its supporting circuitry. The RASTER signal will switch Q6 on and off. This switching will excite the tank circuit formed by the Y yoke and C93, and causes it to oscillate at the same frequency of 41.6 KHz. These raster oscillations will deflect the beam in the Y axis during the alphanumerics mode. This method of generating the raster will cut power consumption in half during the alphanumerics (raster) mode.

3.5.0 ANALOG OUTPUTS

Digital to analog converter, U54, converts the 8 bit data (ID0-ID7) inputs to its analog equivalent at pin 11. The signal is amplified by U68 (pins 12, 13, 14) and fed into pin 3 of U66, a 1 to 8 line data demultiplexer. The three control lines (A, B, C) will demultiplex the input to eight output signals. The sample and hold circuitry will then provide the necessary filtering. The channel one 8/9 high level (CH1 HL) through channel four high level (CH4 HL) are all user programmable outputs. (Refer to Section for more details). The D.A.C. size, D.A.C. offset signals are fed back to adjust the Y-waveform. The intensity signal is routed to the Z-axis board.

3.5.1 HIGH LEVEL OUTPUTS

Four high level outputs are available to the user. These four output ports are located on the 25 pin D-connector, J5, positioned on the back of the unit in the lower left-hand corner. Port 1 is accessed through pin 1, Port 2 through pin 19, Port 3 through pin 6, and Port 4 through Pin 14. Pin 7 of J5 is analog ground. A 25 pin plug assembly designed for use with a flat ribbon cable is available from AMP, Inc: P/N 747321-2. Two 1/2" X 4-40 screws, along with nuts and lock washers, can be used to secure this pin plug assembly to J5.

Each port can be defined by the user in the CONFIG page which can be chosen from the second page of the ESCORT softkeys. Each key has three modes, each with a number of possibilities:

1. The WAVEFORM (WF) mode causes the port to output an ECG waveform or Cardiotach value.

   When an ECG waveform is output, the signal level is approximately 1V/mV and rides on a 2.5V baseline. The selections are as follows:

   ECG1 — The ECG waveform from trace 1 is output.

   ECG2 — The ECG waveform from trace 2 is output.

   ECG3 — The ECG waveform from trace 3 is output.

ECG4 The ECG waveform from trace 4 is output.

When Cardiotach information is output, it is updated every 200ms. 1V = 51 ± 1 BPM, and 2V = 103 ± 1 BPM. The selections are as follows:

HR1 The cardiotach information for trace 1 will be output.

HR2 The cardiotach information for trace 2 will be output.

HR3 The cardiotach information for trace 3 will be ouptut.

HR4 The cardiotach information for trace 4 will be output.

2. The ALARM (ALM) mode can send different alarm conditions to the port. In all the following cases, 0V = no alarm and 5V = alarm condition:

ANY Enables on any alarm condition on any trace.

FLASH Will toggle the port on any alarm condition on any trace.

ECG1 Enables on trace 1 ECG alarm only.

ECG2 Enables on trace 2 ECG alarm only.

ECG3 Enables on trace 3 ECG alarm only.

ECG4 Enables on trace 4 ECG alarm only.

3. In the key mode, the configured output port will enable for approximately 20's as follows:

ANY Enables for 20's when the REC1, REC2, REC3, or REC4 key has been selected.

REC1 Enables for 20's only when REC1 key is selected.

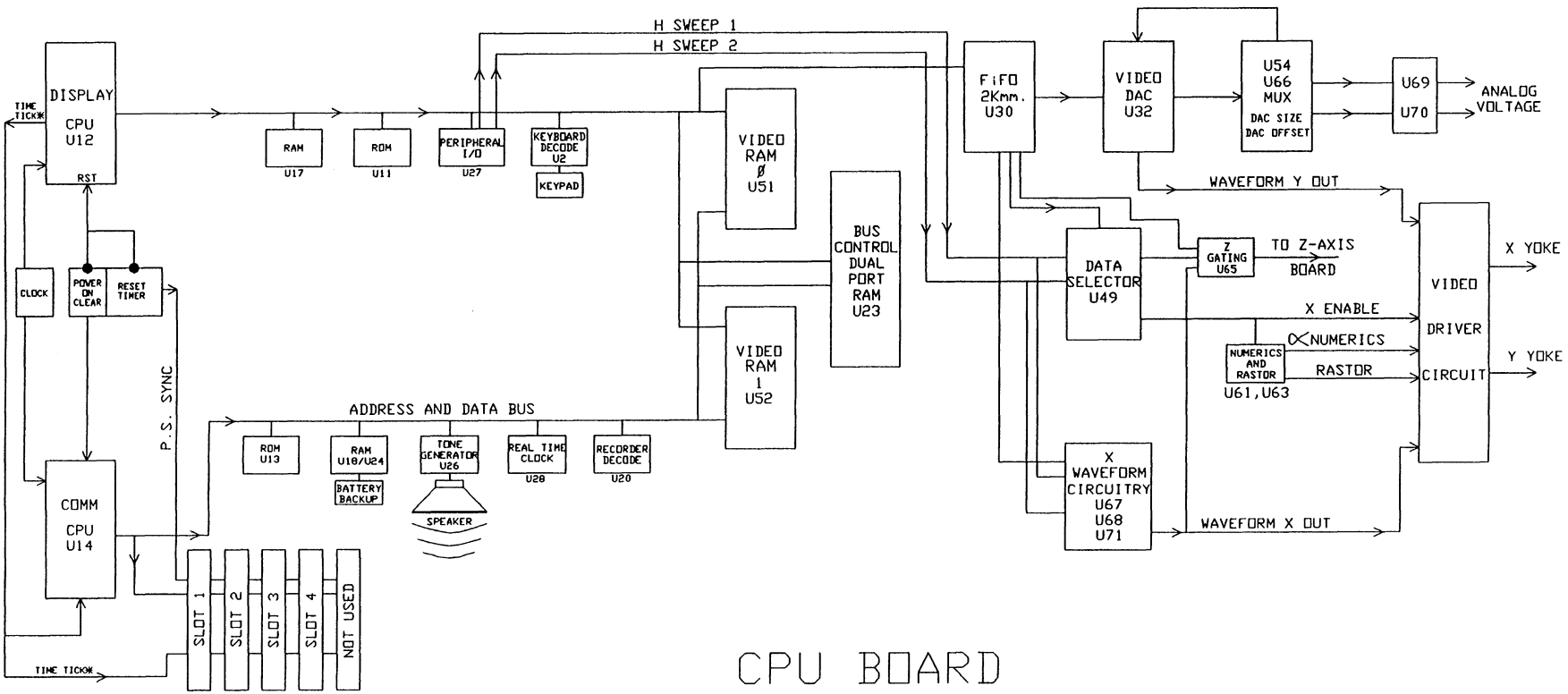
REC2 Enables for 20's only when REC2 key is selected.

REC3 Enables for 20's only when REC3 key is selected.

REC4 Enables for 20's only when REC4 key is selected.

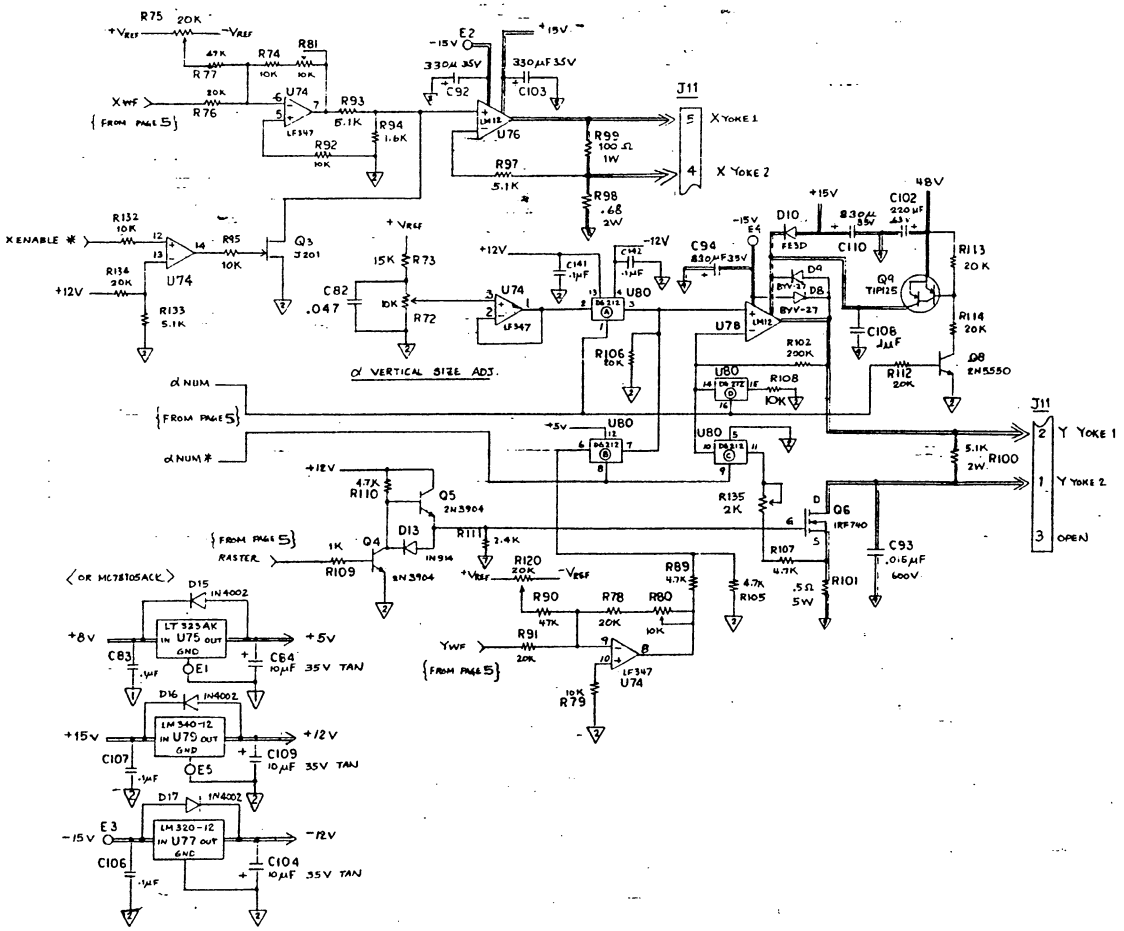
3.6.0 REGULATORS

U75, a 5 volt regulator, is the supply voltage for all digital IC's. U7.9 and U77 are ±12V regulators for supply voltage to various analog IC's. All input voltages for the regulators are supplied from the switching power supply at J12.



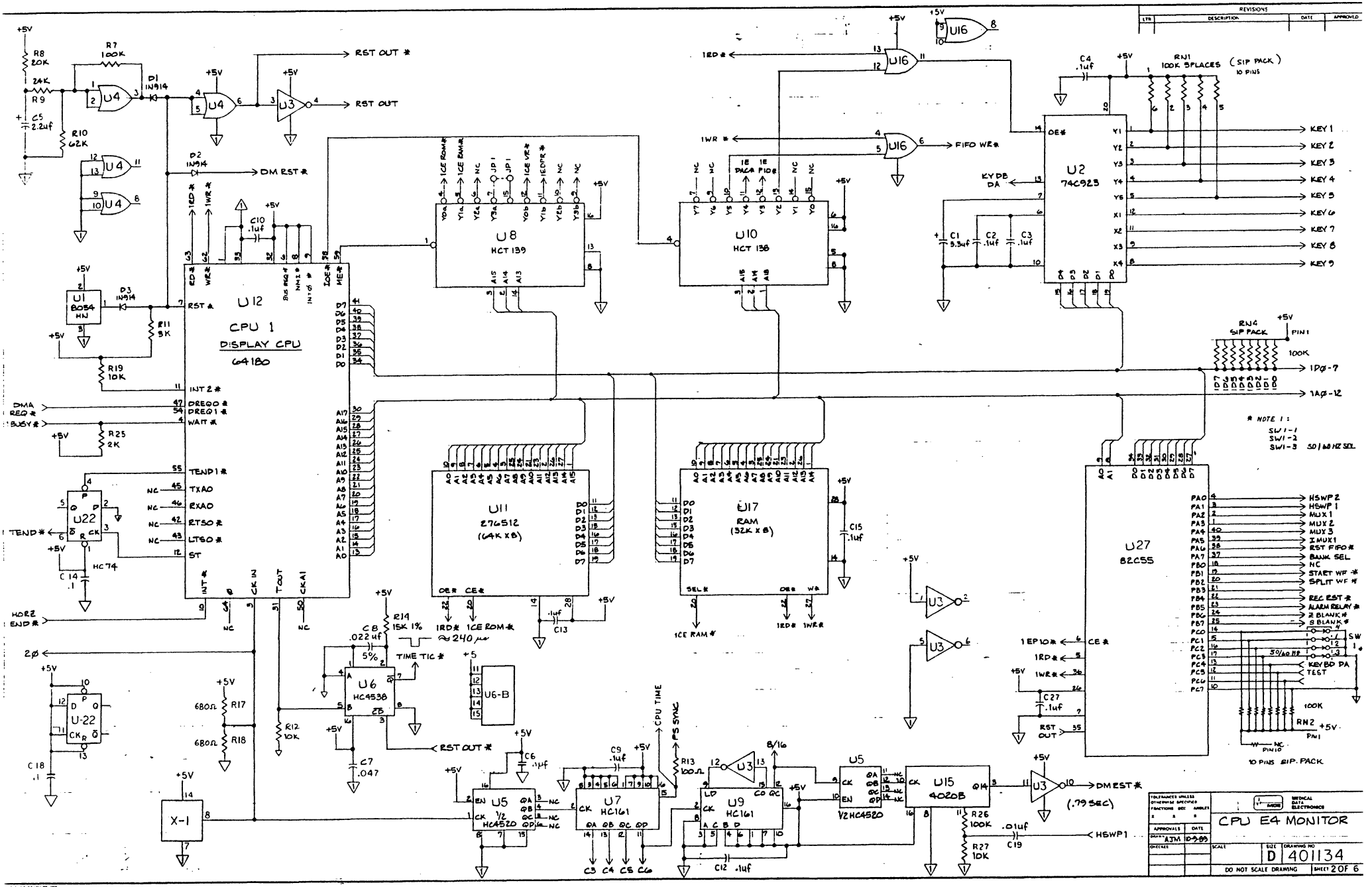
CPU BOARD BLOCK DIAGRAM

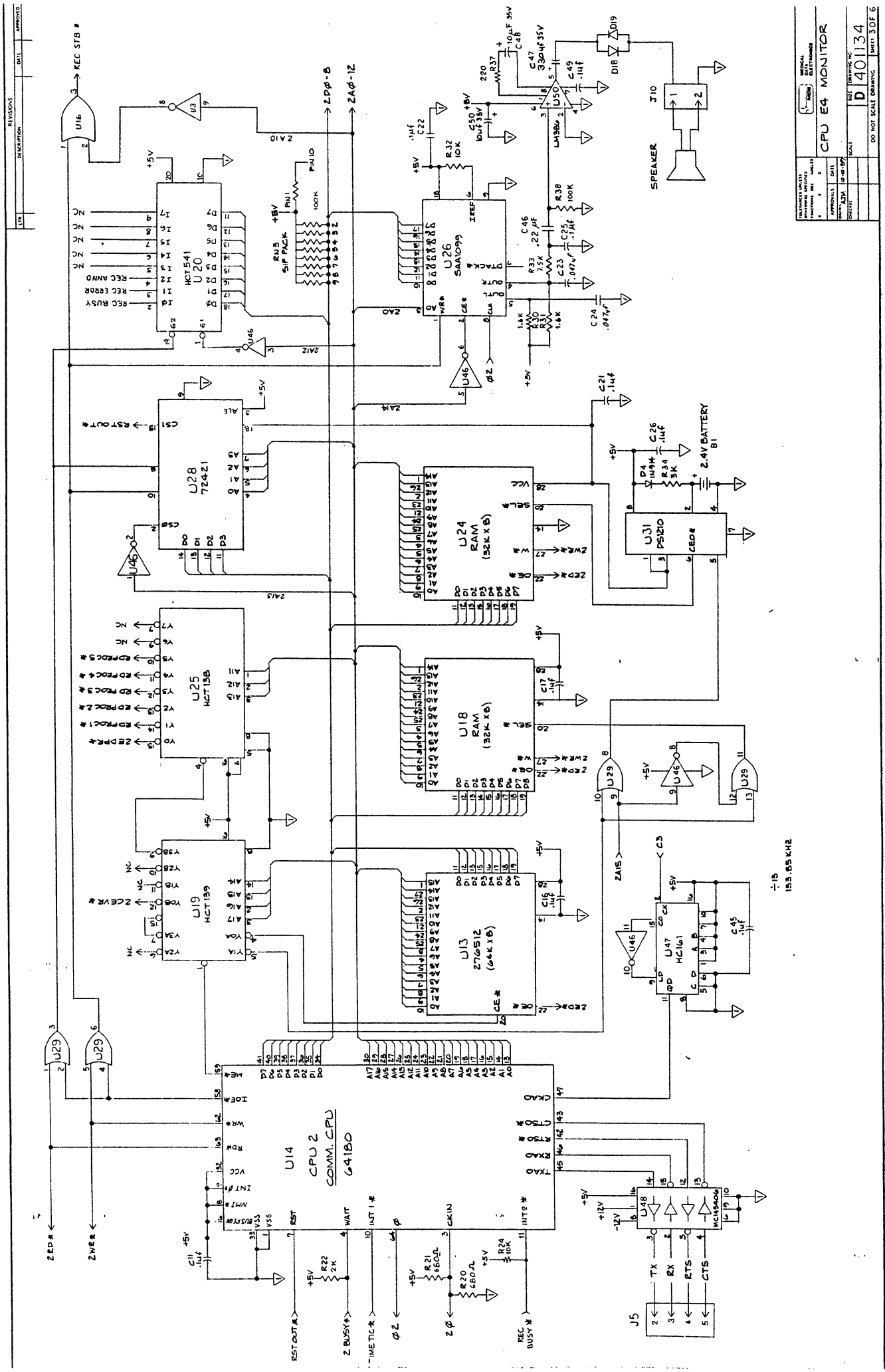
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ECO 689 RELEASE	6-28-1990	
B	ECO 768	10-10-1990	
C	ECO 800	11-16-1990	
D	ECO 897	3-3-1991	

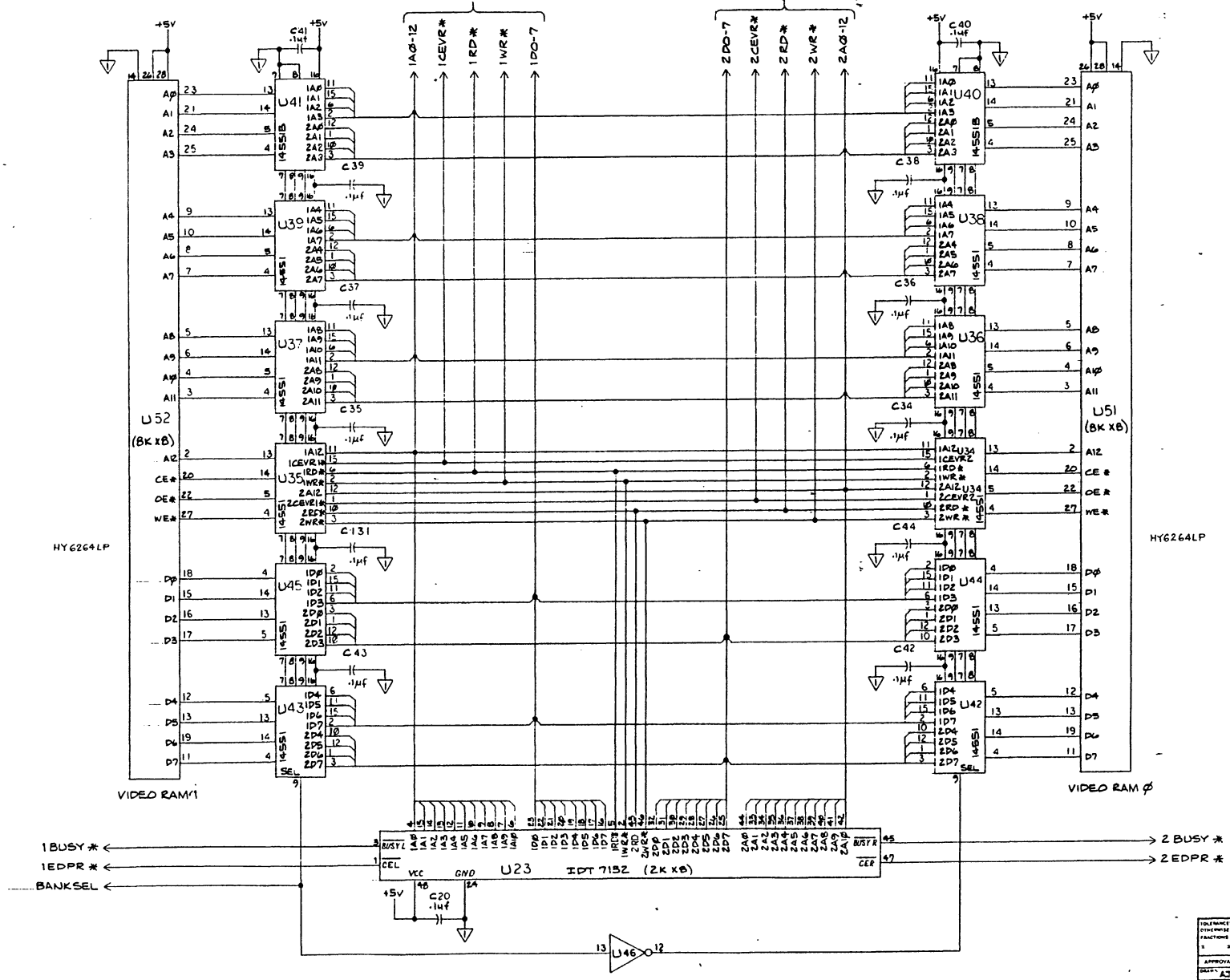


REV:D

TOLERANCES UNLESS OTHERWISE SPECIFIED: FRACTIONS DEC ANGLES		MEDICAL DATA ELECTRONICS
APPROVALS	DATE	CRT DRIVER, CPU 4 CHAN MONITOR
DRAWN		
CHECKED		SCALE: SIZE D DRAWING NO 401134
		DO NOT SCALE DRAWING SHEET 1 OF 6

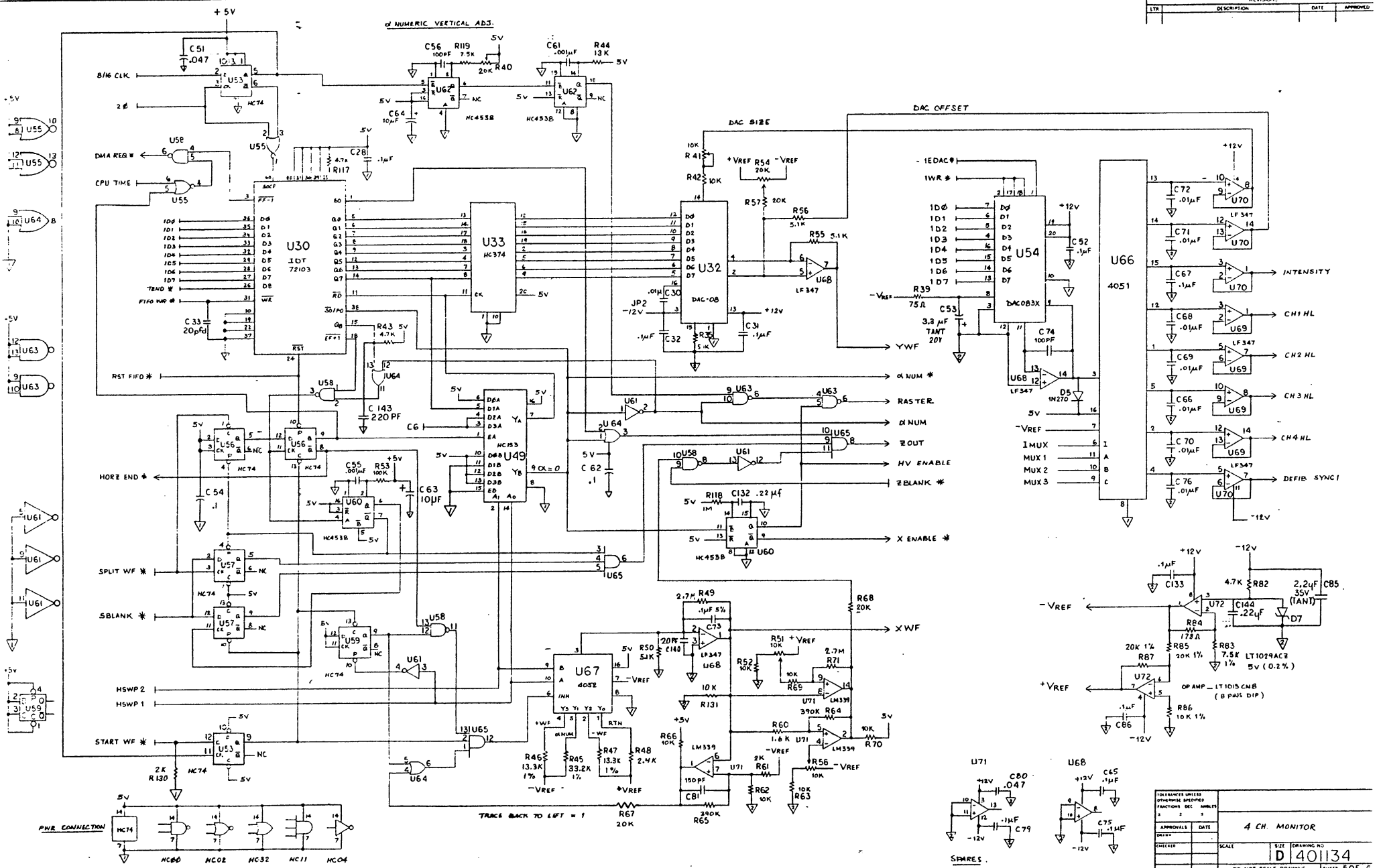

REVISIONS
LTR DESCRIPTION DATE APPROVED
CPU 1
DISPLAY CPU
64180
U12
U2
74C923
U8
HCT 139
U10
HCT 138
U11
27C512
(64K X 8)
U17
RAM
(32K X 8)
U27
82C55
U6
HC4538
U7
HC161
U9
HC161
U15
4020B
U16
U3
U4
U5
U6-B
U22
U1
8084
X-1
RST OUT *
RST OUT
DM RST *
FIFO WR *
KEY 1
KEY 2
KEY 3
KEY 4
KEY 5
KEY 6
KEY 7
KEY 8
KEY 9
RN1 100K 9PLACES (SIP PACK) 10 PINS
RN4 SIP PACK 100K
RN2 100K
1PØ-7
1AØ-12
* NOTE 1 :
SW1-1
SW1-2
SW1-3 50/60 HZ SEL
HSWP2
HSWP1
MUX1
MUX2
MUX3
2 MUX1
RST FIFO *
BANK SEL
NC
START WF *
SPLIT WF *
REC RST *
ALARM RELAY *
2 BLANK *
0 BLANK *
KEYBD PA
TEST
10 PINS SIP PACK
DM EST *
(.79 SEC)
HSWP1
CPU TIME
PS SYNC
TIME TIC *
1RD *
1WR *
1EP10 *
1CE ROM *
1CE RAM *
DMA REQ *
BUSY *
HORZ END *
TEND *
2Ø
KEYB PA
CPU E4 MONITOR
SIZE D
DRAWING NO 401134
SCALE
DO NOT SCALE DRAWING
SHEET 2 OF 6
APPROVALS DATE
DRAWN AJM 10-3-89
CHECKED

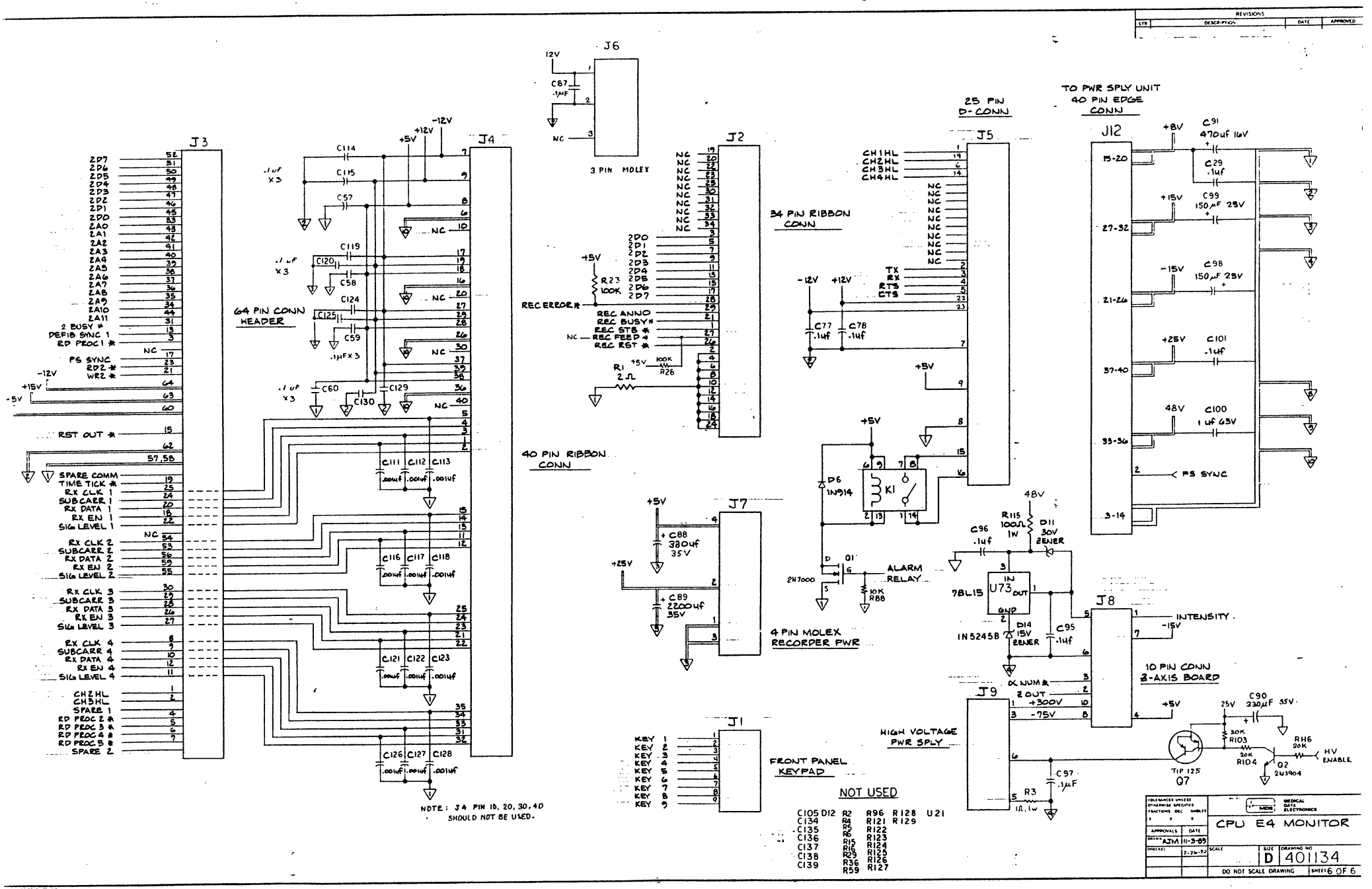

CPU E4 MONITOR
D 401134
SHEET 3 OF 6
DO NOT SCALE DRAWING
SPEAKER
2.4V BATTERY
U14 CPU 2 COMM. CPU 64180
U20 HCT541
U26 SAA1099
U28 72421
U24 RAM (32K x 8)
U18 RAM (32K x 8)
U13 276512 (64K x 8)
U25 HCT138
U19 HCT139
U31 DS1210
U47 HC161
U48 MC1488
U46
U29
U50 LM386
J10
J5
TX
RX
RTS
CTS
÷15
153.85 KHZ

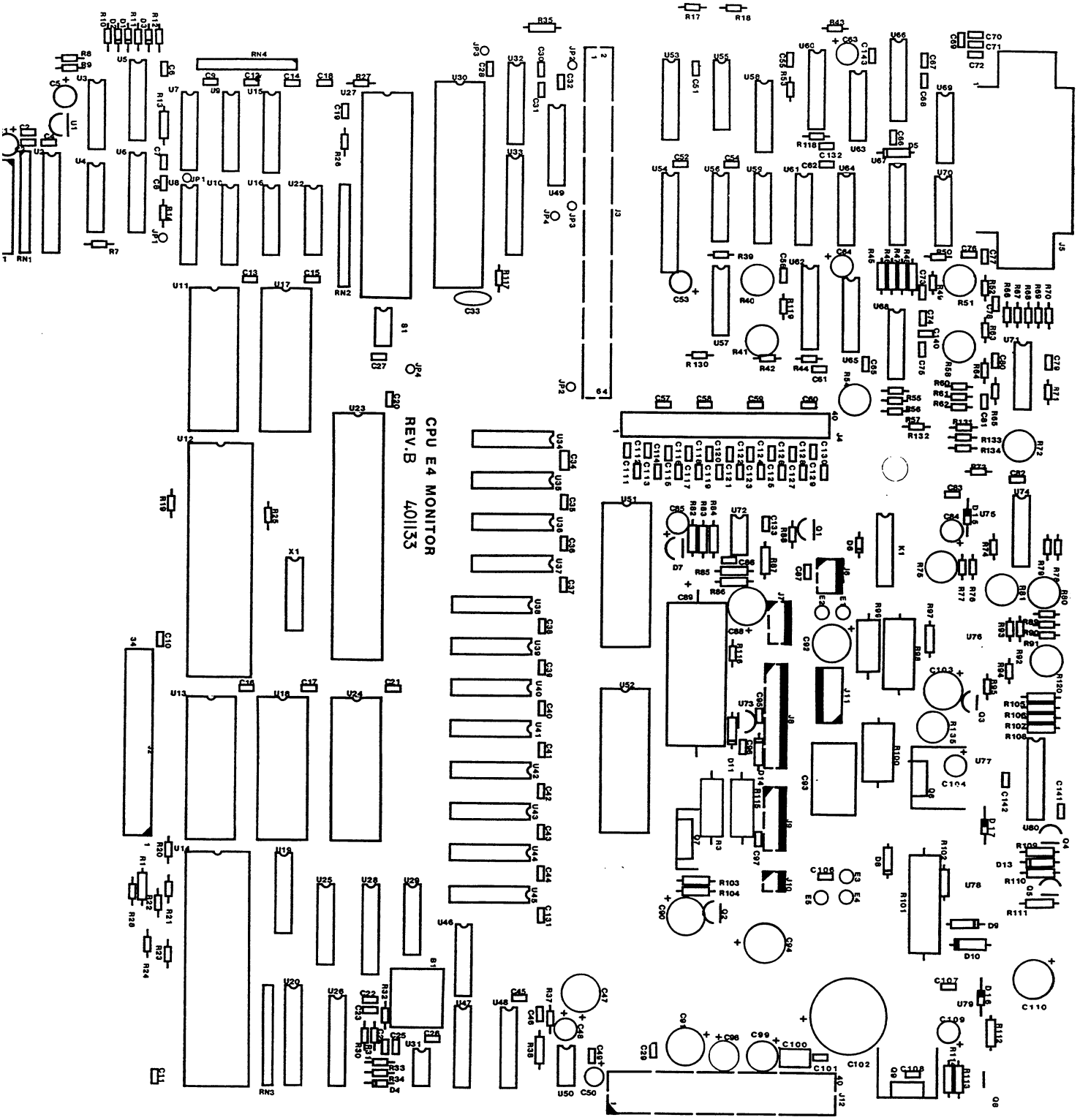


REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES		MEDICAL DATA ELECTRONICS
APPROVALS	DATE	CPU E4 MONITOR
DRAWN AJM	10-11-85	
CHECKED		SIZE D DRAWING NO 401134
		SCALE DO NOT SCALE DRAWING SHEET 4 OF 6


+5V
α NUMERIC VERTICAL ADJ.
8/16 CLK
2Φ
DMA REQ *
CPU TIME
RST FIFO *
HORZ END *
SPLIT WF *
SBLANK *
HSWP 2
HSWP 1
START WF *
PWR CONNECTION
HC00
HC02
HC32
HC11
HC04
U30
IDT 72103
U33
HC374
U32
DAC-08
U54
4051
U66
DAC SIZE
DAC OFFSET
U49
HC153
U67
4052
U68
LF347
U69
U70
U71
LM339
U72
LT1029ACZ
5V (0.2%)
OP AMP — LT1013 CN8 (8 PINS DIP)
YWF
α NUM *
RASTER
α NUM
ZOUT
HV ENABLE
ZBLANK *
X ENABLE *
XWF
INTENSITY
CH1 HL
CH2 HL
CH3 HL
CH4 HL
DEFIB SYNC1
TRACE BACK TO LEFT = 1
SPARES
4 CH. MONITOR
DRAWING NO 401134
SIZE D
SHEET 5OF 6
DO NOT SCALE DRAWING


J3
J4
J6
J2
J5
J12
J7
J1
J8
J9
64 PIN CONN HEADER
40 PIN RIBBON CONN
34 PIN RIBBON CONN
25 PIN D-CONN
TO PWR SPLY UNIT 40 PIN EDGE CONN
4 PIN MOLEX RECORDER PWR
FRONT PANEL KEYPAD
HIGH VOLTAGE PWR SPLY
10 PIN CONN Z-AXIS BOARD
3 PIN MOLEX
ALARM RELAY
NOTE: J4 PIN 10, 20, 30, 40 SHOULD NOT BE USED.
NOT USED
C105 D12 R2 R96 R128 U21
C134 R4 R121 R129
C135 R5 R122
C136 R6 R123
C137 R15 R124
C138 R29 R125
C139 R36 R126
R59 R127
CPU E4 MONITOR
MEDICAL DATA ELECTRONICS
DRAWING NO 401134
SIZE D
SCALE
DO NOT SCALE DRAWING
SHEET 6 OF 6
DRAWN AJM 11-3-89
7-26-90


CPU E4 MONITOR
REV.B 401133

Assembly	Description	Group	PFC	Commodity Class	Planner	Buyer	Drawing	Rev	LT
401134-0000	PCBA, E4 CPU REV. D (E897)			A				D	5

Shrinkage Factor: 0.000

ITEM	LEVEL	SEQ.	DESCRIPTION	REV	CL	LT	QUANTITY	U/M	REFERENCE	MLT	BEGIN	END
401133-0000	*1	1	PCB, E4 CPU REV. B	B	R	33	1.000	EA	-	Yes		
352400-0335A	*1	2	CAP, 3.3UF,20V,20%,RAD,TANT		R	11	2.000	EA	C1,53	Yes		
352300-0104A	*1	3	CAP, .1UF,50V,20%,RAD,MYLAR		R	22	8.000	EA	C,2,3,4,6,9,10,11,12	Yes		
352300-0104A	*1	4	CAP, .1UF,50V,20%,RAD,MYLAR		R	22	7.000	EA	C13,14,15,16,17,18,20	Yes		
352300-0104A	*1	5	CAP, .1UF,50V,20%,RAD,MYLAR		R	22	7.000	EA	C21,22,25,26,27,28,31	Yes		
352300-0104A	*1	6	CAP, .1UF,50V,20%,RAD,MYLAR		R	22	7.000	EA	C32,34,35,36,37,38,39	Yes		
352300-0104A	*1	7	CAP, .1UF,50V,20%,RAD,MYLAR		R	22	7.000	EA	C40,41,42,43,44,45,49	Yes		
352300-0104A	*1	8	CAP, .1UF,50V,20%,RAD,MYLAR		R	22	7.000	EA	C52,54,60,62,65,67,75	Yes		
352300-0104A	*1	9	CAP, .1UF,50V,20%,RAD,MYLAR		R	22	7.000	EA	C77,78,79,83,86,87,95	Yes		
352300-0104A	*1	10	CAP, .1UF,50V,20%,RAD,MYLAR		R	22	5.000	EA	C96,97,101,106,107	Yes		
352300-0104A	*1	11	CAP, .1UF,50V,20%,RAD,MYLAR		R	22	5.000	EA	C108,114,115,119,120	Yes		
352300-0104A	*1	12	CAP, .1UF,50V,20%,RAD,MYLAR		R	22	5.000	EA	C124,125,129,130,131	Yes		
352300-0104A	*1	13	CAP, .1UF,50V,20%,RAD,MYLAR		R	22	6.000	EA	C133,141,142,29,57,58	Yes		
352300-0104A	*1	14	CAP, .1UF,50V,20%,RAD,MYLAR		R	22	1.000	EA	C59	Yes		
352300-0103A	*1	15	CAP, .01UF,50V,20%,RAD,MYLAR		R	22	7.000	EA	C19,30,66,68,69,70,71	Yes		
352300-0103A	*1	16	CAP, .01UF,50V,20%,RAD,MYLAR		R	22	2.000	EA	C72,76	Yes		
352300-0102A	*1	17	CAP, 1000PF,50V,20%,RAD,MYLAR		R	22	5.000	EA	C55,111,112,113,116	Yes		
352300-0102A	*1	18	CAP, 1000PF,50V,20%,RAD,MYLAR		R	22	5.000	EA	C117,118,121,122,123	Yes		
352300-0102A	*1	19	CAP, 1000PF,50V,20%,RAD,MYLAR		R	22	3.000	EA	C126,127,128	Yes		
352401-0225A	*1	20	CAP, 2.2UF,35V,20%,TANT		R	11	2.000	EA	C5,85	Yes		
352202-0337A	*1	21	CAPACITOR, RADIAL, 330UF, 35V, 10X16MM, ELECTROL.		R	22	6.000	EA	C47,88,92,103,90,94	Yes		
352401-0106A	*1	22	CAP, 10UF,35V,20%,RAD,TANT		R	11	5.000	EA	C48,50,63,64,84	Yes		
352401-0106A	*1	23	CAP, 10UF,35V,20%,RAD,TANT		R	11	2.000	EA	C104,109	Yes		
352600-0022A	*1	24	CAP, 20PF,50V,CER DISC,NP0		R	11	2.000	EA	C33,140	Yes		

Assembly	Description	Group	PFC	Commodity Class	Planner	Buyer	Drawing	Rev	LT
401134-0000	PCBA, E4 CPU REV. D (E897)			A				D	5

Shrinkage Factor: 0.000

ITEM	LEVEL	SEQ.	DESCRIPTION	REV	CL	LT	QUANTITY	U/M	REFERENCE	MLT	BEGIN	END
352300-0473A	*1	25	CAP, .047UF,50V,20%,MYLAR		R	22	6.000	EA	C7,23,24,51,80,82	Yes		
352100-0151A	*1	26	CAP, 150PF,25V,10%,RAD,X7R		R	22	1.000	EA	C81	Yes		
352100-0101A	*1	27	CAP, 100PF,25V,10%,RAD,NP0		R	11	2.000	EA	C56,74	Yes		
352300-0224A	*1	28	CAP, .22UF,50V,20%,MYLAR		R	22	2.000	EA	C46,132	Yes		
352301-0105A	*1	29	CAP, 1UF,63V,20%,MYLAR		R	22	1.000	EA	C100	Yes		
352101-0102A	*1	30	CAP,NPO DIELECTRIC, 1000PF (.001UF),5%,50V,RAD, .1		R	22	1.000	EA	C61	Yes		
352202-0337A	*1	31	CAPACITOR, RADIAL, 330UF, 35V, 10X16MM, ELECTROL.		R	22	1.000	EA	C110	Yes		
352200-0477A	*1	32	CAP, 470UF,16V,ELECT, RAD		R	22	1.000	EA	C91	Yes		
352200-0157A	*1	33	CAP, 150uF,25V,20%,RAD,ELECT,8mm x 12mm		R	22	2.000	EA	C98,99	Yes		
352201-0228A	*1	34	CAP, 2200UF,35V,AX,ELECT, 16X30MM		R	66	1.000	EA	C89	Yes		
352301-0104A	*1	35	CAP, .1UF,5%,MYLAR		R	66	1.000	EA	C73	Yes		
352600-0028A	*1	36	CAP, .015uF,600V,POLYPROPYLENE		R	44	1.000	EA	C93	Yes		
352204-0227A	*1	37	CAP, 220uF,63V,LOW ESR,ELECT		R	33	1.000	EA	C102	Yes		
370100-0020A	*1	38	RES, 2,1/4W,5%,CF		R	11	1.000	EA	R1	Yes		
370100-0472A	*1	39	RES, 4.7K,1/4W,5%,CF		R	11	4.000	EA	R82,105,107,110	Yes		
370101-0681A	*1	40	RES, 680,1/8W,5%,CF		R	11	4.000	EA	R17,18,20,21	Yes		
370101-0202A	*1	41	RES, 2K,1/8W,5%,CF		R	11	4.000	EA	R22,25,61,130	Yes		
370101-0472A	*1	42	RES, 4.7K,1/8W,5%,CF		R	11	3.000	EA	R43,89,117	Yes		
370101-0302A	*1	43	RES, 3K,1/8W,5%,CF		R	11	2.000	EA	R11,34	Yes		
370101-0103A	*1	44	RES, 10K,1/8W,5%,CF		R	11	7.000	EA	R12,19,24,27,32,42,52	Yes		
370101-0103A	*1	45	RES, 10K,1/8W,5%,CF		R	11	6.000	EA	R62,131,132,63,66,69	Yes		
370101-0103A	*1	46	RES, 10K,1/8W,5%,CF		R	11	6.000	EA	R70,79,88,92,95,74	Yes		
370101-0153A	*1	47	RES, 15K,1/8W,5%,CF		R	11	1.000	EA	R73	Yes		
370100-0102A	*1	48	RES, 1K,1/4W,5%,CF		R	11	1.000	EA	R109	Yes		

Assembly	Description	Group	PFC	Commodity Class	Planner Buyer	Drawing	Rev	LT
01134-0000	PCBA, E4 CPU REV. D (E897)			A			D	5

Shrinkage Factor: 0.000

ITEM	LEVEL	SEQ.	DESCRIPTION	REV	CL	LT	QUANTITY	U/M	REFERENCE	MLT	BEGIN	END
370100-0101A	*1	49	RES, 100,1/4W,5%,CF		R	11	1.000	EA	R13	Yes		
370101-0221A	*1	50	RES, 220,1/8W,5%,CF		R	11	1.000	EA	R37	Yes		
370101-0512A	*1	51	RES, 5.1K,1/8W,5%,CF		R	11	5.000	EA	R50,55,56,93,133	Yes		
370101-0203A	*1	52	RES, 20K,1/8W,5%,CF		R	11	7.000	EA	R8,57,78,67,68,76,91	Yes		
370101-0203A	*1	53	RES, 20K,1/8W,5%,CF		R	11	2.000	EA	R116,134	Yes		
370101-0752A	*1	54	RES, 7.5K,1/8W,5%,CF		R	11	2.000	EA	R33,119	Yes		
370100-0203A	*1	55	RES, 20K,1/4W,5%,CF		R	11	5.000	EA	R103,104,106,112,113	Yes		
370100-0203A	*1	56	RES, 20K,1/4W,5%,CF		R	11	1.000	EA	R114	Yes		
370100-0242A	*1	57	RES, 2.4K,1/4W,5%,CF		R	11	2.000	EA	R48,111	Yes		
370101-0623A	*1	58	RES, 62K,1/8W,5%,CF		R	11	1.000	EA	R10	Yes		
370200-1332A	*1	59	RES, 13.3K,1/4W,1%,MF		R	11	2.000	EA	R46,47	Yes		
370200-3322A	*1	60	RES, 33.2K,1/4W,1%,MF		R	11	1.000	EA	R45	Yes		
370101-0473A	*1	61	RES, 47K,1/8W,5%,CF		R	11	2.000	EA	R77,90	Yes		
370101-0104A	*1	62	RES, 100K,1/8W,5%,CF		R	11	5.000	EA	R23,26,28,53,7	Yes		
370101-0204A	*1	63	RES, 200K,1/8W,5%,CF		R	11	1.000	EA	R102	Yes		
370101-0394A	*1	64	RES, 390K,1/8W,5%,CF		R	11	2.000	EA	R64,65	Yes		
370101-0243A	*1	65	RES, 24K,1/8W,5%,CF		R	11	1.000	EA	R9	Yes		
370101-0105A	*1	66	RES, 1M,1/8W,5%,CF		R	11	1.000	EA	R118	Yes		
364000-0130A	*1	67	IC, LF347 (SCREENED TO + /- 1.5mV), NATIONAL ONLY		A	22	1.000	EA	U68	Yes		
370101-0275A	*1	68	RES, 2.7M,1/8W,5%,CF		R	11	3.000	EA	R40,71,49	Yes		
370201-0101A	*1	69	RES, 100,1W,METAL OXIDE		R	11	2.000	EA	R99,115	Yes		
370200-1002A	*1	70	RES, 10K,1/4W,1%,MF		R	11	1.000	EA	R86	Yes		
370200-7501A	*1	71	RES, 7.5K,1/4W,1%,MF		R	11	1.000	EA	R83	Yes		
370200-1780A	*1	72	RES, 178,1/4W,1%,MF		R	11	1.000	EA	R84	Yes		

Assembly	Description	Group	PFC	Commodity Class	Planner Buyer	Drawing	Rev	LT
401134-0000	PCBA, E4 CPU REV. D (E897)			A			D	5

Shrinkage Factor: 0.000

ITEM	LEVEL	SEQ.	DESCRIPTION	REV	CL	LT	QUANTITY	U/M	REFERENCE	MLT	BEGIN	END
370200-2002A	*1	73	RES, 20K,1/4W,1%,MF		R	11	2.000	EA	R85,87	Yes		
370100-0104A	*1	74	RES, 100K,1/4W,5%,CF		R	11	1.000	EA	R38	Yes		
370100-0512A	*1	75	RES, 5.1K,1/4W,5%,CF		R	11	2.000	EA	R35,97	Yes		
352100-0221A	*1	76	CAP, 220PF,10%,X7R,.1 L.S		R	22	1.000	EA	C143 (TO U64, PIN 13)	Yes		
370101-0133A	*1	77	RES, 13K,1/8W,5%,CF		R	11	1.000	EA	R44	Yes		
370101-0750A	*1	78	RES, 75,1/8W,5%,CF		R	11	1.000	EA	R39	Yes		
370100-0103A	*1	79	RES, 10K,1/4W,5%,CF		R	11	1.000	EA	R108	Yes		
370203-6800A	*1	80	RES, 0.68,2W,M.O.		R	33	1.000	EA	R98	Yes		
370203-5000A	*1	81	RES, 0.5,5W,M.O.		R	33	1.000	EA	R101	Yes		
370203-0512A	*1	82	RES, 5.1K,2W,5%,750V,TYPE HB		R	33	1.000	EA	R100	Yes		
374000-0103A	*1	83	POT, 10K,TRIM,TOP ADJ,OFF CTR LEADS,CERMET		R	11	6.000	EA	R41,51,58,72,80,81	Yes		
374000-0203A	*1	84	POT, 20K,TRIM,TOP ADJ,OFF CTR LEADS,CERMET		R	11	4.000	EA	R40,54,75,120	Yes		
374100-0202A	*1	85	POT, 2K,TRIM,TOP ADJ,CTRD LEADS,CERMET		R	11	1.000	EA	R135	Yes		
370300-0003A	*1	86	RES, SIP,100K,10P,NTWK,9		R	11	4.000	EA	RN1,2,3,4	Yes		
378000-0005A	*1	87	DIO, 1N914,SIGNAL T&R		R	11	6.000	EA	D1,2,3,4,6,13	Yes		
378000-0001A	*1	88	DIO, 1N270 T&R		R	11	1.000	EA	D5	Yes		
378000-0031A	*1	89	DIO, FE3D,200V,3A,ULTRAFAST-2ND OP PREP ARGOSY		R	11	1.000	EA	D10	Yes		
378000-0030A	*1	90	DIO, 1N4751A,30V,1W,5%,ZENER T&R ***MOT ONLY***		R	11	1.000	EA	D11	Yes		
378000-0041A	*1	91	DIO, BYV27-150 (OR -200) T&R		R	22	2.000	EA	D8,9	Yes		
378000-0002A	*1	92	DIO, 1N4002GP,RCTFR, (MOT ONLY) T&R		R	11	3.000	EA	D15,16,17	Yes		
378000-0043A	*1	93	DIO, LT1029ACZ,5V,PRES		R	22	1.000	EA	D7	Yes		
378000-0047A	*1	94	DIO, 1N5245,15V,ZENER **MOT ONLY**		R	33	1.000	EA	D14	Yes		
360600-0010A	*1	95	HTSNK, 5768B		R	11	2.000	EA	HS1,2	Yes		
376000-0019A	*1	97	XSTR, 2N7000,FET		R	11	1.000	EA	Q1	Yes		

Assembly	Description	Group	PFC	Commodity Class	Planner	Buyer	Drawing	Rev	LT
401134-0000	PCBA, E4 CPU REV. D (E897)			A				D	5

Shrinkage Factor: 0.000

ITEM	LEVEL	SEQ.	DESCRIPTION	REV	CL	LT	QUANTITY	U/M	REFERENCE	MLT	BEGIN	END
376000-0003A	*1	98	XSTR, 2N3904		R	11	3.000	EA	Q2,4,5	Yes		
376000-0018A	*1	99	XSTR, 2N5550,NPN SILICON(VCE 140V)		R	11	6.050	EA		Yes		
376000-0010A	*1	100	XSTR, TIP 125,DARLINGTON PWR XSTR		R	11	2.000	EA	Q7,9	Yes		
376000-0020A	*1	101	XSTR, J201,FET		R	11	1.000	EA	Q3	Yes		
376000-0024A	*1	102	XSTR, IRF740,MOSFET		R	33	1.000	EA	Q6	Yes		
364000-0124A	*1	103	I.C., S-8054 ALR, TO 92 P KG., VOLT.DET. 4.3 TO 4.6		R	22	1.000	EA	U1	Yes		
364000-0173A	*1	104	IC, LF347 SCREENED FROM - 0009, -0130, -0135		A	5	3.000	EA	U69,70,74	Yes		
364000-0010A	*1	105	IC, LM339		R	11	1.000	EA	U71	Yes		
364000-0111A	*1	106	IC, 78L15 +15V REG.		R	11	1.000	EA	U73	Yes		
364000-0025A	*1	107	IC, 74HC04		R	11	3.000	EA	U3,46,61	Yes		
364000-0027A	*1	108	IC, 74HC32		R	11	4.000	EA	U4,16,29,64	Yes		
364000-0031A	*1	109	IC, 74HC161		R	11	3.000	EA	U7,9,47	Yes		
364000-0104A	*1	110	IC, 74HC139		R	11	2.000	EA	U8,19	Yes		
364000-0029A	*1	111	IC, 74HC138		R	11	2.000	EA	U10,25	Yes		
364000-0102A	*1	112	IC, 27C512, EPROM, 200NS		R	11	2.000	EA	U11,13	Yes		
364000-0092A	*1	113	IC, HD 64180 RP-8 (Z180-8 MHZ)		R	11	2.000	EA	U12,14	Yes		
364000-0103A	*1	114	IC, 4020B		R	11	1.000	EA	U15	Yes		
364000-0105A	*1	115	IC, TL55257 PL12 32 X 8 RAM, STATIC		R	11	3.000	EA	U17,18,24	Yes		
364000-0028A	*1	116	IC, 74HC74		R	11	5.000	EA	U22,53,56,57,59	Yes		
364000-0095A	*1	117	IC, MS6132,DUAL PORT RAM, 8 X 2K,48-PIN (OR MS7132)		R	11	1.000	EA	U23	Yes		
364000-0101A	*1	118	IC, 82C55 **MITSUBISHI ON LY**		R	22	1.000	EA	U27	Yes		
364000-0123A	*1	119	IC, RTC 72421A		R	22	1.000	EA	U28	Yes		
364000-0106A	*1	120	IC, DS1210		R	11	1.000	EA	U31	Yes		
364000-0097A	*1	121	IC, 74HC374		R	11	1.000	EA	U33	Yes		

Assembly	Description	Group	PFC	Commodity Class	Planner Buyer	Drawing	Rev	LT
401134-0000	PCBA, E4 CPU REV. D (E897)			A			D	5

Shrinkage Factor: 0.000

ITEM	LEVEL	SEQ.	DESCRIPTION	REV	CL	LT	QUANTITY	U/M	REFERENCE	MLT	BEGIN	END
364000-0048A	*1	122	IC, DAC-08CP		R	11	1.000	EA	U32	Yes		
364000-0100A	*1	123	IC, MC145406		R	11	1.000	EA	U48	Yes		
364000-0007A	*1	124	IC, HM6264LP-15,150NS (OR HM6264LP-12,120NS)		R	44	2.000	EA	U51,52	Yes		
364000-0002A	*1	125	IC, DAC-083X, NOTE: X = EITHER 0, 1, OR 2.		R	11	1.000	EA	U54	Yes		
364000-0024A	*1	126	IC, 74HC00		R	11	2.000	EA	U58,63	Yes		
364000-0121A	*1	127	IC, 74HC11		R	22	1.000	EA	U65	Yes		
364000-0040A	*1	128	IC, 4051		R	11	1.000	EA	U66	Yes		
364000-0055A	*1	129	IC, CD4052		R	11	1.000	EA	U67	Yes		
364000-0008A	*1	130	IC, DG212CJ		R	11	1.000	EA	U80	Yes		
370101-0162A	*1	132	RES, 1.6K,1/8W,5%,CF		R	11	4.000	EA	R30,31,60,94	Yes		
364000-0154A	*1	135	IC, LM386N-1,LOW VOLT,1W, OP AMP		R	33	1.000	EA	U50	Yes		
364000-0155A	*1	136	IC, 74C923		R	33	1.000	EA	U2	Yes		
364000-0156A	*1	137	IC, 74HC4520		R	33	1.000	EA	U5	Yes		
364000-0157A	*1	138	IC, 74HC4538		R	33	3.000	EA	U6,60,62	Yes		
364000-0158A	*1	139	IC, 74HCT541		R	33	1.000	EA	U20	Yes		
364000-0159A	*1	140	IC, SAA1099P		R	33	1.000	EA	U26	Yes		
364000-0160A	*1	141	IC, IDT72103, FIFO		R	33	1.000	EA	U30	Yes		
364000-0161A	*1	142	IC, 74HC153		R	33	1.000	EA	U49	Yes		
364000-0162A	*1	143	IC, LT1013 CN8 OP AMP (8-POS DIP)		R	33	1.000	EA	U72	Yes		
364000-0163A	*1	144	IC, 74HC02		R	33	1.000	EA	U55	Yes		
364000-0164A	*1	145	IC, MC14551		R	33	6.000	EA	U34,35,36,37,38,39	Yes		
364000-0164A	*1	146	IC, MC14551		R	33	6.000	EA	U40,41,42,43,44,45	Yes		
380000-0020A	*1	147	SW, 8-PIN DIP		R	33	1.000	EA	SW1	Yes		
356000-0021A	*1	148	XTAL, 16MHZ OSC IC		R	33	1.000	EA	X1	Yes		

ssembly	Description	Group	PFC	Commodity	Class	Planner	Buyer	Drawing	Rev	LT
01134-0000	PCBA, E4 CPU REV. D (E897)				A				D	5

hrinkage Factor: 0.000

ITEM	LEVEL	SEQ.	DESCRIPTION	REV	CL	LT	QUANTITY	U/M	REFERENCE	MLT	BEGIN	END
384000-0036A	*1	149	BATT, 2.4V (1 PIN NEG; 2 PINS POS.)		R	11	1.000	EA	B1		Yes	
380000-0014A	*1	150	RELAY, DIP (REED), 6V COIL RESISTANCE, 500/600 OHM		R	22	1.000	EA	K1		Yes	
365000-0008A	*1	151	SKT, 8-POS,DIP,TIN PLATE, L.P.		R	11	3.000	EA			Yes	
365000-0014A	*1	152	SKT, 14-POS,DIP,TIN PLATE ,L.P.		R	11	21.000	EA			Yes	
365000-0016A	*1	153	SKT, 16-POS,DIP,TIN PLATE ,L.P.		R	11	30.000	EA			Yes	
365000-0018A	*1	154	SKT, 18-POS,DIP,TIN PLATE ,L.P.		R	11	2.000	EA			Yes	
365000-0020A	*1	155	SKT, 20-POS,DIP, TIN PLATE,L.P.		R	11	3.000	EA			Yes	
365000-0028A	*1	156	SKT, 28-POS,DIP,TIN PLATE ,L.P.		R	11	7.000	EA			Yes	
365000-0040A	*1	157	SKT, 40-POS,DIP,TIN PLATE ,L.P.		R	11	2.000	EA			Yes	
365000-0064A	*1	158	SKT, 64-PIN,.07 LEADS		R	11	2.000	EA			Yes	
354000-0103A	*1	161	CONN, SGL ROW,STRT,SGL PINS,SNAP-AWAY		R	11	9.000	PIN	J1		Yes	
354000-0106A	*1	162	CONN, DBL ROW,STRT,SGL PIN,SNAP-AWAY		R	11	34.000	PIN	J2		Yes	
354000-0106A	*1	163	CONN, DBL ROW,STRT,SGL PIN,SNAP-AWAY		R	11	40.000	PIN	J4		Yes	
354000-0008A	*1	164	CONN, 25-PIN,F,R/A		R	11	1.000	EA	J5		Yes	
354000-0148A	*1	165	CONN, 4-P,M,STRT,.1 CTR,LOCKING RAMP		R	11	1.000	EA	J7		Yes	
354000-0033A	*1	166	CONN, 10-PIN,M,STRT LCK,.1 CTR		R	11	1.000	EA	J8		Yes	
354000-0138A	*1	167	CONN, 2-P,M,STRT LOCK,.1 CTR,HDR		R	11	1.000	EA	J10		Yes	
354000-0084A	*1	168	CONN, 3-P,M,STRT LCK,.1 CTR		R	11	1.000	EA	J6		Yes	
354000-0146A	*1	169	CONN, 40-PIN,CARD EDGE,.1 CTR,.437-.460 HIGH		R	22	1.000	EA	J12		Yes	
354000-0031A	*1	170	CONN, 5-P,M,STRT LOCK,.1 CTR		R	11	1.000	EA	J11		Yes	
354000-0210A	*1	171	CONN, 64-PIN,F,DBL ROW,STRT HDR		R	33	1.000	EA	J3		Yes	
354000-0211A	*1	172	CONN, 6-PIN,M,STRT,0.1" CTR		R	33	1.000	EA	J9		Yes	
370201-0010A	*1	173	RES, 1,1W,METAL OXIDE		R	11	1.000	EA	R3		Yes	
352300-0014A	*1	174	CAP, .022UF,5%,MYLAR		R	77	1.000	EA	C8		Yes	

ssembly	Description	Group	PFC	Commodity Class	Planner Buyer	Drawing	Rev	LT
01134-0000	PCBA, E4 CPU REV. D (E897)				A		D	5

hrinkage Factor: 0.000

ITEM	LEVEL	SEQ.	DESCRIPTION	REV	CL	LT	QUANTITY	U/M	REFERENCE	MLT	BEGIN	END
370202-1502A	*1	175	RES, 15K,1/8W,1%		R	11	1.000	EA	R14	Yes		
365000-0148A	*1	176	SOCKET, 48 PIN DIP		R	22	1.000	EA		Yes		
358100-0010A	*1	177	SCR, 4-40 X 1/2,PH PNHD,C AD1 ONLY		R	11	4.000	EA	DO NOT ISSUE	Yes		
358100-0036A	*1	178	SCR, 4-40 X 1/4,PH PNHD,C AD2 OR ANY		R	11	6.000	EA	DO NOT ISSUE	Yes		
358200-0002A	*1	179	WSHR, #4 FLT FIBER (4X5/1 6X3/64)		R	11	8.000	EA	DO NOT ISSUE	No		
358200-0009A	*1	180	WSHR, #4 SPLIT LOCK		R	11	10.000	EA	DO NOT ISSUE	Yes		
401136-0000	*1	181	PCBA, INTERFACE E4 REV. A (E689)		A	5	1.000	EA		Yes		
401229-0000	*1	182	COUPLER ASSY, E4 REV. A1 (D056)	A1	A	33	1.000	EA		Yes		
352300-0015A	*1	183	CAP, .22UF,10%,MYLAR		R	66	1.000	EA	C144	Yes		
378000-0036A	*1	184	DIO, 1N5819,1AMP,SCHOTTKY T&R		R	11	2.000	EA	D18,19	Yes		

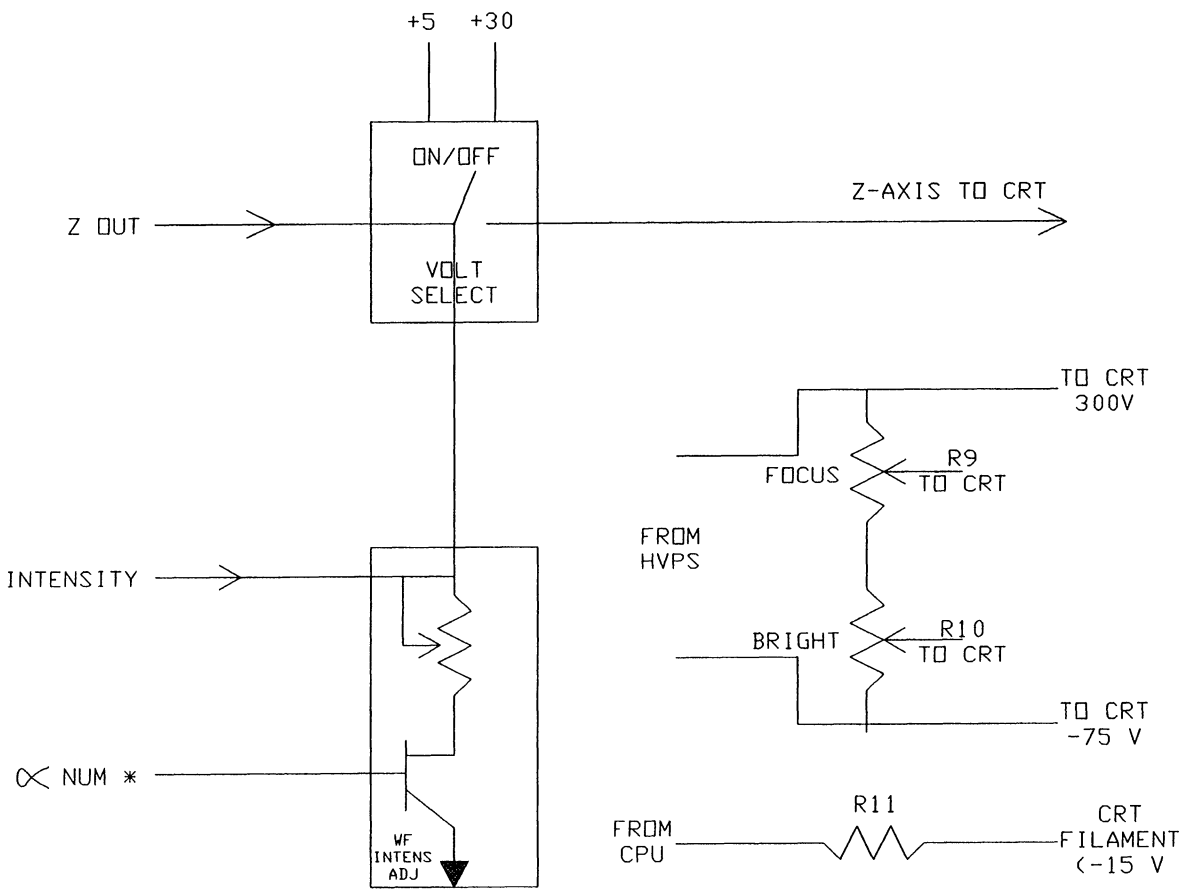
Cumulative Lead Time for 401134-0000 = 82

Z-AXIS BOARD

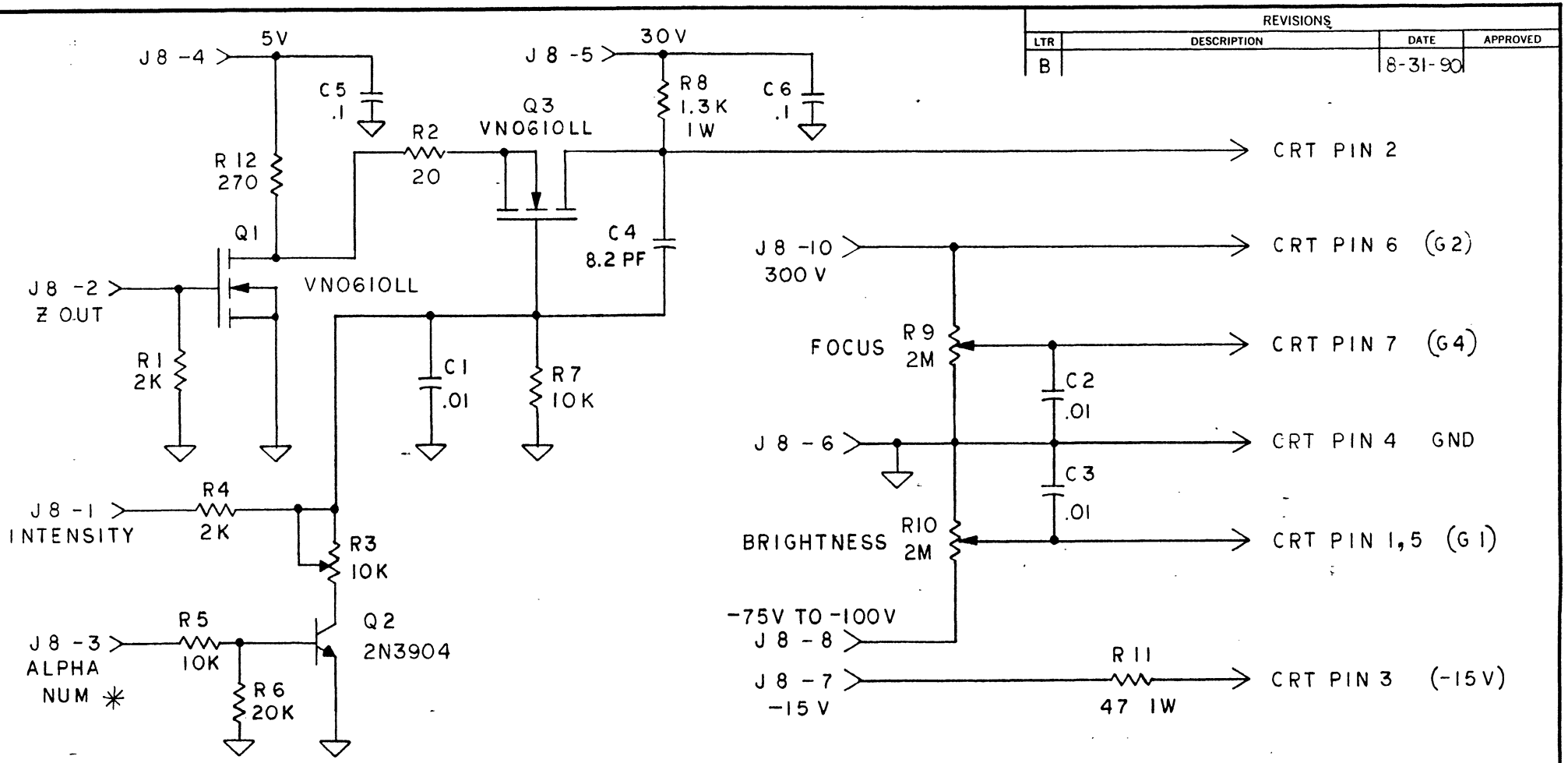
CHAPTER 4

4.0.0 Z-AXIS BOARD

The Z-axis board handles all the voltages needed to bias the CRT. Q3 controls the biasing of the CRT cathode (CRT pin 2). During the waveform mode Q3 is employed as a variable resistor with the drain to source resistance being varied by the amount of gate biasing. Waveform mode gate biasing is set by the intensity signal (J8-1), R4, R3 and Q2. R3 varies the amount of biasing which will in turn vary the intensity of the four waveforms on the screen. In the alphanumeric mode, gate biasing of Q3 is set by the intensity signal through voltage divider R4 and R7. R9 varies the Grid 4 voltage (CRT, pin 7) for focus control of the screen. R10 is the Grid 1 (CRT pin 1, 5) control which sets the overall brightness of the screen. CRT, pin 3 is the filament (heater) voltage.



Z-AXIS BLOCK DIAGRAM



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
B		8-31-90	

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

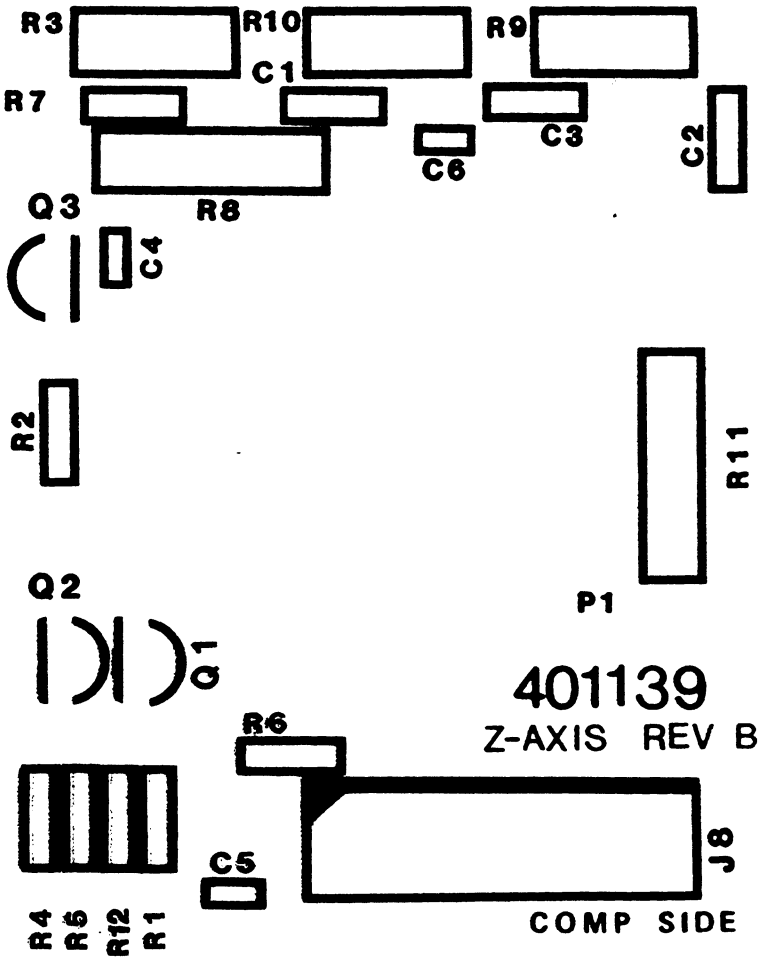
APPROVALS	DATE
DRAWN SDM	6 29
CHECKED	
	90

Z AXIS BOARD

SCALE	SIZE	DRAWING NO.
	B	401140

DO NOT SCALE DRAWING — SHEET 1 OF 2

BISHOP GRAPHICS INC
REORDER NO 20621


R3
R10
R9
C1
R7
C3
C2
C6
R8
Q3
C4
R2
R11
P1
Q2
Q1
401139
Z-AXIS REV B
R6
J8
C5
R4
R5
R12
R1
COMP SIDE

Assembly	Description	Group	PFC	Commodity Class	Planner Buyer	Drawing	Rev	LT
401140-0000	PCBA, Z-AXIS, E4 REV. C			A			C	5

Shrinkage Factor: 0.000

ITEM	LEVEL	SEQ.	DESCRIPTION	REV	CL	LT	QUANTITY	U/M	REFERENCE	MLT	BEGIN	END
401139-0000	*1	1	PCB, Z-AXIS E4 REV. B (E732)		R	33	1.000	EA	-	Yes		
352600-0019A	*1	2	CAP, .01UF,1000V,20%,Z5U, CER DISC,.4 L.S.		R	11	3.000	EA	C1, C2, C3	Yes		
352600-0009A	*1	3	CAP, 8.2PF,50V,+/-.5PF,RAD,CER		R	22	1.000	EA	C4	Yes		
376000-0003A	*1	4	XSTR, 2N3904		R	11	1.000	EA	Q2	Yes		
365000-0149A	*1	5	CRT SOCKET, 7 PIN PC MOUNT WITH SPARK GAP E4		R	22	1.000	EA	P1	Yes		
352300-0104A	*1	6	CAP, .1UF,50V,20%,RAD,MYLAR		R	22	2.000	EA	C5,6	Yes		
370100-0200A	*1	7	RES, 20,1/4W,5%,CF		R	11	1.000	EA	R2	Yes		
370100-0103A	*1	8	RES, 10K,1/4W,5%,CF		R	11	2.000	EA	R5,7	Yes		
370100-0202A	*1	9	RES, 2K,1/4W,5%,CF		R	11	2.000	EA	R1,4	Yes		
370201-0132A	*1	10	RES, 1.3K,1W,5%.M.O.		R	22	1.000	EA	R8	Yes		
374300-0205A	*1	11	POT, 2M,TRIM,SIDE ADJ,CERMET,3/8 SQR,.15LS		R	11	2.000	EA	R9, R10	Yes		
370201-0470A	*1	12	RES, 47,1W,METAL OXIDE		R	11	1.000	EA	R11	Yes		
370100-0271A	*1	13	RES, 270,1/4W,5%,CF		R	11	1.000	EA	R12	Yes		
376000-0026A	*1	14	TRANSISTOR, FET N CHANNEL VN0610LL SILICONIX ONLY		R	22	2.000	EA	Q1,3	Yes		
354000-0033A	*1	15	CONN, 10-PIN,M,STRT LCK,.1 CTR		R	11	1.000	EA	J8	Yes		
374300-0103A	*1	16	POT, 10K,TRIM,SIDE ADJ,CERMET,3/8 IN.QR,.15LS		R	11	1.000	EA	R3	Yes		
370100-0203A	*1	17	RES, 20K,1/4W,5%,CF		R	11	1.000	EA	R6	Yes		

Cumulative Lead Time for 401140-0000 = 38

DIGITAL SUBCARRIER BOARD

CHAPTER 5

5.0.0 DIGITAL SUBCARRIER BOARD

5.1.0 OVERVIEW

The Digital Subcarrier Board in the **ESCORT 400** provides a universal method of decoding various biomedical telemetry signals from a wide variety of transmitter manufacturers.

The input subcarrier signal is received in an analog format, then is turned into a digital signal. This digitized signal has the subcarrier portion of the signal removed leaving only the digital ECG. The digital representation of the ECG waveform is then sent to the CPU Board for further processing.

This board is also responsible to dispatch to the receiver the data it needs to configure itself to the appropriate TV band and manufacturer type currently being received.

5.2.0 MICROPROCESSOR

A Z-80 type microprocessor is used on the digital subcarrier board. Xtal Y1, an 8 MHz oscillator, is divided by two for a 4 MHz clock signal to drive the microprocessor, U6. RESET* comes in from the CPU Board to reset the processor at pin 26. Pins 17 and 25 are tied high and not used. INTR* at pin 16 will interrupt the processor when the required amount of cycles has been counted by the timers, U7, U9, and U11. The address and data buses communicate data to and from the timers, dual port RAM and ROM as well as other chips. The signal WAIT* at pin 23 inserts wait states to the dual port RAM. Memory request (MR*), write (WR*), read (RD*) and I/O outputs at pins 19-22 are decoded by U15 for the control signals memory read (MRRD*), memory write (MRWR*), I/O write (IOWR*), and I/O read (IORD*).

5.2.1 EPROM, AND DUAL PORT RAM

U8, an 8 X 64K EPROM, is enabled through U16 which decodes A11-A15. That along with memory read (MRRD*) at pin 22 will put the EPROM data on the bus. The same signal, inverted through U17, will enable U13, the dual port RAM. The dual port RAM interfaces the digital subcarrier board to the CPU Board. Data is written to and read from the CPU Board through the edge connector.

5.2.2 DECODERS

U10 decodes address lines A5, A6, A7 for the chip enable signals I/O 1-7. These signals, along with IORD* and IOWR*, will enable various functions throughout the board. U14 decodes for the signals LEVEL SELECT, FLT SEL (filter select) and GATE 0-2. U14 also interfaces to the receiver by sending data to indicate what first FM frequency to decode in the FM/FM demodulation. U5 decodes for the signal GAIN SELECT, which goes to U21 pin 5.

5.2.3 VOLTAGE REGULATORS

U20 and U22 regulate the +10 volts and -10 volts. The voltages are then filtered by C23, C24, C39 and C40.

5.2.4 AMPLIFICATION OF SIGNAL

The subcarrier input (SUB CAR) from the receiver enters the subcarrier board from the edge connector through the CPU Board. the signal enters a variable gain stage comprised of U21 and Q8. The signal GAIN SELECT at U21 pin 5 will adjust the gain stage either high or low depending on the selected manufacturer. The ability to vary the gain eliminates the possibility of clipping the signal and losing information.

5.2.5 THREE CHANNEL FILTERING

The amplified signal then goes to a three channel filtering stage. All three filters are similar in operation, but have a different bandwidth. Which filter is used is dependent on the manufacturer and what parameter is being decoded. For simplicity we will discuss the F1OUT filter located in the center of the schematics.

5.2.6 SWITCHED CAPACITOR FILTERS

R4 and C2 pre-filter the signal. U24 and U2 are switched capacitor filters whose bandpass center frequency is dependent on the clock input at pin 3, (F1CLK). By putting the filters in series, the bandpass is sharpened. The output at U2 pin 2 then goes through a low pass filter to remove any signal from the clock that was input to U24 and U2. The sinewave is then turned into a squarewave by U4, a high gain amplifier, with the edges sharpened by U18 and Q4. The subcarrier signal has now become a digital squarewave, (F1OUT), that can be processed and further decoded.

Aside from the filter circuit just described, the center filter, F1OUT, has additional circuitry. The signal filter select, FLT SEL, is used to lower the bandpass of the filter circuit at the output of U2. The switched capacitor filter is used for detecting auxiliary parameters such as remote record and low battery signals which can be transmitted at very low frequencies. If one of these functions is being looked at, the bandpass center frequency is lowered by turning Q1 and Q2 on. This will put C11 and C12 in parallel with C9 and C10, lowering the cutoff frequency and removing any clock signal that may have entered the subcarrier signal.

The signal LEVEL SELECT puts R43 in parallel with R15 by turning on Q7. This reduces hystersis and will make the comparator, U4, more sensitive when it is looking for small signals like pacers.

Then to reduce noise on the signal, Q7 will switch off and only a large signal will cause U4 to switch high and low.

5.2.7 TIMERS

U7, U9, and U11 are all high performance CMOS programmable interval timers. Each has three independently programmable 16 bit counters. U7 acts as a function generator to the switched capacitor filters, U1, U2, U3, U23, U24, and U25. The microprocessor will program U7 for the appropriate frequency output at pins 10, 13 and 17, (F0CLK, F1CLK, and F2CLK), depending on the selected manufacturer and other parameters. The clock output will be 54.5 times the center frequency required of the switched capacitor filters.

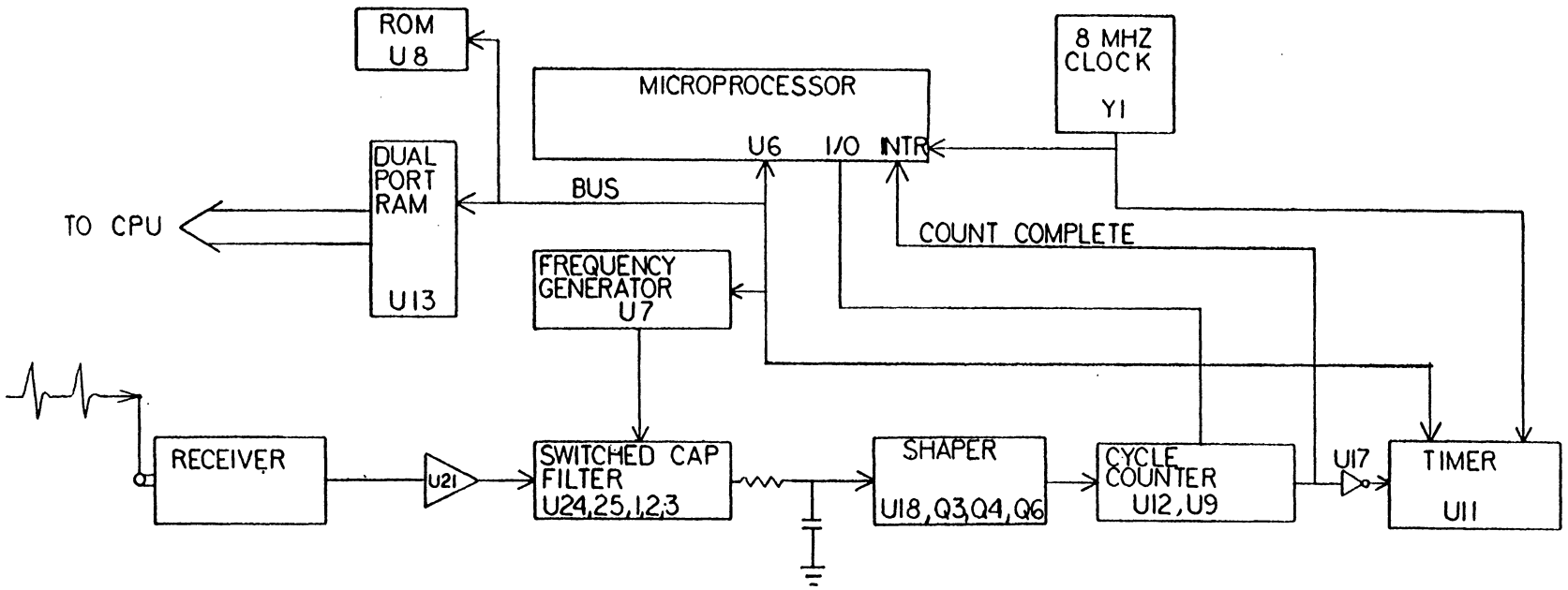
The U9 timer is responsible for counting "cycles". One cycle is equal to the space between positive edges of the square wave. The signals GATE 0-2 will tell U9 to begin counting on the next positive edge of the input at pins 9, 15, and 18, (F0OUT, F1OUT, F2OUT). At this time the outputs, OUT 0-2, will go low to indicate the start of the count. This data goes to U11, after being inverted at U17, which will start counting.

U11's function is to count 8 MHz clocks during the period of time set by the microprocessor called a sample. When the prescribed number of cycles has been counted, the outputs of U9 will go high to signify the end of the sample being taken. This will signal U12, PAL, which will interrupt the microprocessor, (INTR*), to retrieve the data from U11.

This "time counted" along with the number of "cycles counted" is used to calculate the incoming subcarrier frequency.

Once the data has been retrieved, the processor will automatically reset the timers to count the next data sample. The processor then must keep track of where the incoming frequency is, compared to the manufacturers selected center frequency, to determine the actual ECG waveform.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

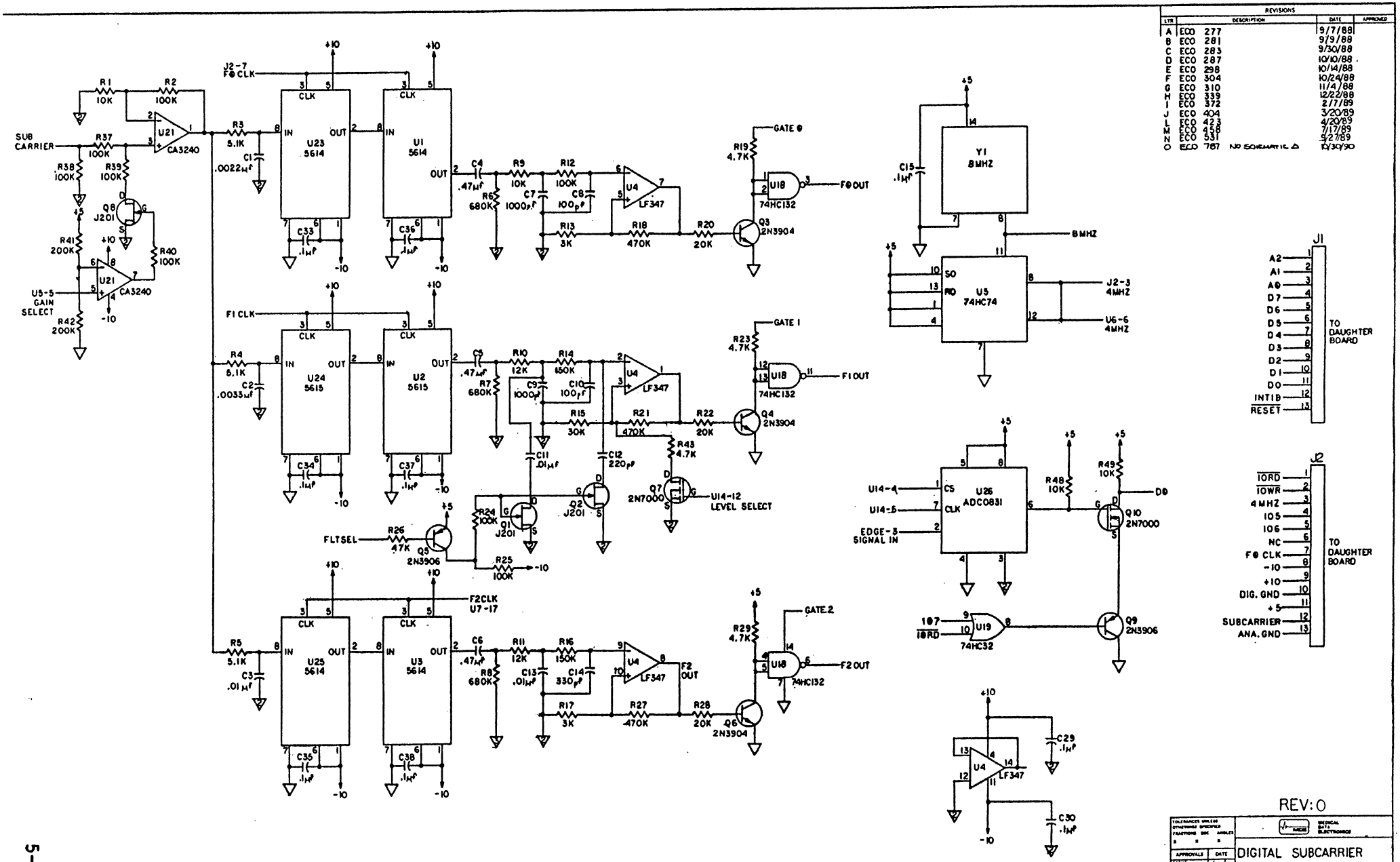
APPROVALS	DATE
DRAWN A. Krause	11-7-88
CHECKED	

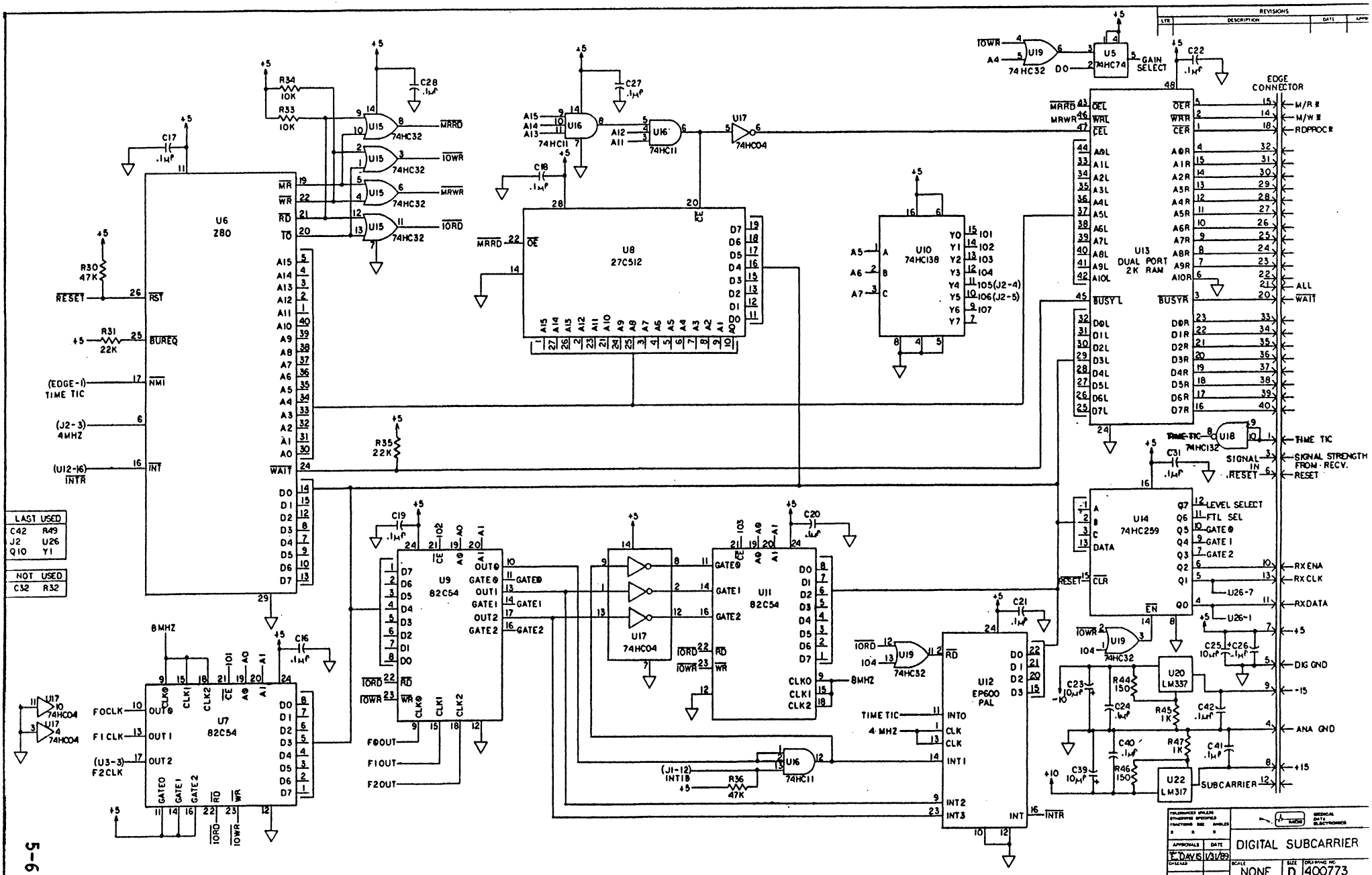
MEDICAL DATA ELECTRONICS

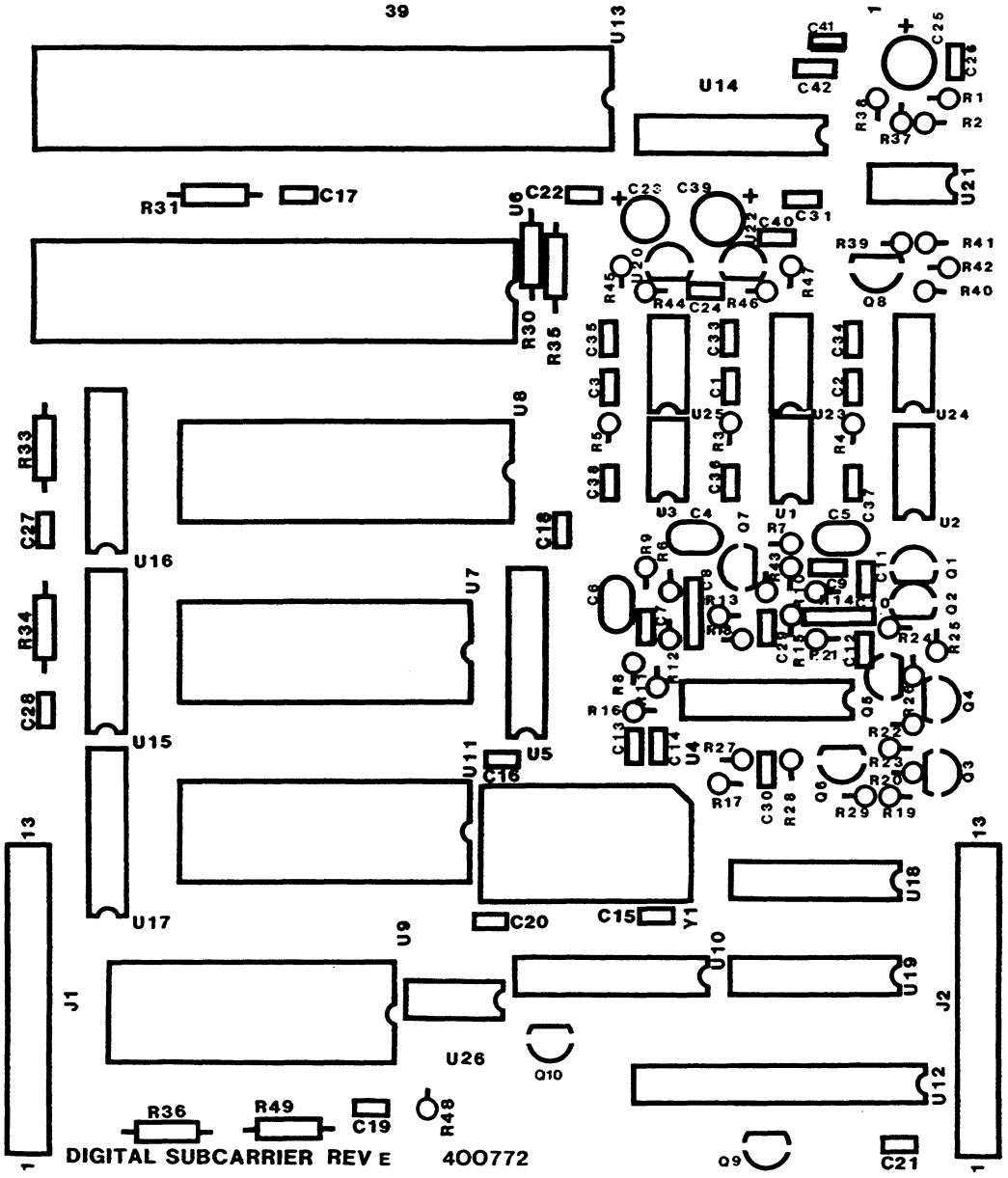
DIGITAL SUBCARRIER BOARD
BLOCK DIAGRAM

SCALE	SIZE	DRAWING NO.
Ø	B	

DO NOT SCALE DRAWING | SHEET 1 OF 1


REVISIONS
LTR DESCRIPTION DATE APPROVED
A ECO 277 9/7/88
B ECO 281 9/9/88
C ECO 283 9/30/88
D ECO 287 10/10/88
E ECO 298 10/14/88
F ECO 304 10/24/88
G ECO 310 11/4/88
H ECO 339 12/22/88
I ECO 372 2/7/89
J ECO 404 3/20/89
K ECO 423 4/20/89
L ECO 458 7/17/89
M ECO 531 9/27/89
N ECO 787 NO SCHEMATIC Δ 10/30/90
SUB CARRIER
U5-5 GAIN SELECT
J2-7 FØ CLK
F1 CLK
F2CLK U7-17
FLTSEL
U14-4
U14-5
EDGE-3 SIGNAL IN
U14-12 LEVEL SELECT
GATE Ø
GATE 1
GATE 2
FØ OUT
F1 OUT
F2 OUT
8MHZ
J2-3 4MHZ
U6-6 4MHZ
TO DAUGHTER BOARD
A2
A1
A0
D7
D6
D5
D4
D3
D2
D1
D0
INTIB
RESET
IORD
IOWR
4MHZ
I05
I06
NC
FØ CLK
-10
+10
DIG. GND
+5
SUBCARRIER
ANA. GND
DØ
U1 5614
U2 5615
U3 5614
U23 5614
U24 5615
U25 5614
U26 ADC0831
U5 74HC74
U18 74HC132
U19 74HC32
U4 LF347
Y1 8MHZ
Q1 J201
Q2 J201
Q3 2N3904
Q4 2N3904
Q5 2N3906
Q6 2N3904
Q7 2N7000
Q8 J201
Q9 2N3906
Q10 2N7000
U21 CA3240
R1 10K
R2 100K
R3 5.1K
R4 5.1K
R5 5.1K
R6 680K
R7 680K
R8 680K
R9 10K
R10 12K
R11 12K
R12 100K
R13 3K
R14 150K
R15 30K
R16 150K
R17 3K
R18 470K
R19 4.7K
R20 20K
R21 470K
R22 20K
R23 4.7K
R24 100K
R25 100K
R26 47K
R27 470K
R28 20K
R29 4.7K
R37 100K
R38 100K
R39 100K
R40 100K
R41 200K
R42 200K
R43 4.7K
R48 10K
R49 10K
C1 .0022μf
C2 .0033μf
C3 .01μf
C4 .47μf
C5 .47μf
C6 .47μf
C7 1000pf
C8 100pf
C9 1000pf
C10 100pf
C11 .01μf
C12 220pf
C13 .01μf
C14 330pf
C15 .1μf
C29 .1μf
C30 .1μf
C33 .1μf
C34 .1μf
C35 .1μf
C36 .1μf
C37 .1μf
C38 .1μf
+10
-10
+5
CLK
IN
OUT
TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
APPROVALS DATE
DRAWN F DAVIS 2/7/89
CHECKED
MEDICAL DATA ELECTRONICS
DIGITAL SUBCARRIER
SCALE NONE
SIZE D
DRAWING NO 400773
DO NOT SCALE DRAWING
SHEET 1 OF 2
REV: 0


U6 Z80
U8 27C512
U10 74HC138
U13 DUAL PORT 2K RAM
U14 74HC259
U12 EP600 PAL
U9 82C54
U11 82C54
U7 82C54
U5 74HC74
U15 74HC32
U16 74HC11
U17 74HC04
U18 74HC132
U19 74HC32
U20 LM337
U22 LM317
R30 47K
R31 22K
R33 10K
R34 10K
R35 22K
R36 47K
R44 150
R45 1K
R46 150
R47 1K
C17 .1µF
C18 .1µF
C19 .1µF
C20 .1µF
C21 .1µF
C22 .1µF
C23 10µF
C24 .1µF
C25 10µF
C26 .1µF
C27 .1µF
C28 .1µF
C31 .1µF
C39 10µF
C40 .1µF
C41 .1µF
C42 .1µF
RESET
BUREQ
(EDGE-1) TIME TIC
(J2-3) 4MHZ
(U12-16) INTR
8MHZ
FOCLK
F1CLK
(U3-3) F2CLK
F0OUT
F1OUT
F2OUT
(J1-12) INT1B
TIME TIC
4 MHZ
GAIN SELECT
EDGE CONNECTOR
M/R*
M/W*
RDPROC*
ALL
WAIT
TIME TIC
SIGNAL STRENGTH FROM RECV.
RESET
LEVEL SELECT
FTL SEL
GATE0
GATE 1
GATE 2
RXENA
RXCLK
RXDATA
DIG GND
-15
ANA GND
+15
SUBCARRIER
INTR
LAST USED
C42 R49
J2 U26
Q10 Y1
NOT USED
C32 R32
DIGITAL SUBCARRIER
NONE
D
400773
DO NOT SCALE DRAWING
SHEET 2 OF
9-5


39
1
U13
U14
C41
C42
C25
C26
R1
R2
R37
R38
U21
R31
C17
U6
C22
C23
C39
C31
C40
R39
R41
R42
R40
Q8
R30
R35
C35
C33
C34
U8
U25
U23
U24
U3
U1
U2
C4
C5
C37
Q7
Q1
Q2
U16
U7
U5
C16
U11
U15
U17
U18
C20
C15
Y1
U9
U10
U19
J1
J2
U26
Q10
U12
R36
R49
C19
R48
Q9
C21
DIGITAL SUBCARRIER REV E 400772

Assembly	Description	Group	PFC	Commodity	Class	Planner	Buyer	Drawing	Rev	LT
400773-0000	PCBA, 200MHZ DIGITAL SUBC., E2 REV. '01'(D055)				A				01	0

Shrinkage Factor: 0.000

ITEM	LEVEL	SEQ.	DESCRIPTION	REV	CL	LT	QUANTITY	U/M	REFERENCE	MLT	BEGIN	END
352300-0104A	*1	1	CAP, .1UF,50V,20%,RAD,MYLAR		R	22	5.000	EA	C15,16,18,19,20,	Yes		
352300-0104A	*1	2	CAP, .1UF,50V,20%,RAD,MYLAR		R	22	6.000	EA	C21,22,24,26,27,28,	Yes		
352300-0104A	*1	3	CAP, .1UF,50V,20%,RAD,MYLAR		R	22	6.000	EA	C29,30,31,35,38,40	Yes		
352100-0104A	*1	4	CAP, .1UF,50V,10%,RAD,X7R		R	11	7.000	EA	C36,37,33,34,17,41,42	Yes		
352300-0474A	*1	5	CAP, .47UF, 50V,20%,RAD,MYLAR(METALLIZED POLYESTR)		R	22	3.000	EA	C4,5,6	Yes		
352100-0101A	*1	6	CAP, 100PF,25V,10%,RAD,NP0		R	11	2.000	EA	C8,10	Yes		
352300-0102A	*1	7	CAP, 1000PF,50V,20%,RAD,MYLAR		R	22	2.000	EA	C7,9	Yes		
352300-0103A	*1	8	CAP, .01UF,50V,20%,RAD,MYLAR		R	22	3.000	EA	C3,11,13	Yes		
352100-0221A	*1	9	CAP, 220PF,10%,X7R,.1 L.S.		R	22	1.000	EA	C12	Yes		
352300-0222A	*1	10	CAP, 2200PF,50V OR 100V,1%,MYLAR,.15L.S.		R	77	1.000	EA	C1	Yes		
352100-0331A	*1	11	CAP, 330PF,25V,10%,RAD,X7R		R	22	1.000	EA	C14	Yes		
352300-0332A	*1	12	CAP, .0033UF,50V,20%,RAD, MYLAR,.1 L.S.		R	22	1.000	EA	C2	Yes		
352401-0106A	*1	13	CAP, 10UF,35V,20%,RAD,TANT		R	11	3.000	EA	C23,25,39	Yes		
354000-0171A	*1	14	CONN, 13-SKT STRP,.1CTR,.335HT		R	11	2.000	EA	J1,2	Yes		
356000-0015A	*1	15	REFERENCE OSCILLATOR 8MHZ		R	22	1.000	EA	Y1	Yes		
364000-0004A	*1	16	IC, CA3240		R	11	1.000	EA	U21	Yes		
364000-0173A	*1	17	IC, LF347 SCREENED FROM -0009, -0130, -0135		A	5	1.000	EA	U4	Yes		
364000-0025A	*1	18	IC, 74HC04		R	11	1.000	EA	U17	Yes		
364000-0027A	*1	19	IC, 74HC32		R	11	2.000	EA	U15,19	Yes		
364000-0028A	*1	20	IC, 74HC74		R	11	1.000	EA	U5	Yes		
364000-0029A	*1	21	IC, 74HC138		R	11	1.000	EA	U10	Yes		
364000-0064A	*1	22	IC, LM317LZ,VOLT. REGULATOR		R	11	1.000	EA	U22	Yes		
364000-0080A	*1	23	IC, TMPZ84C00P (Z80A, CMOS VERSION)		R	11	1.000	EA	U6	Yes		
364000-0095A	*1	24	IC, MS6132,DUAL PORT RAM, 8 X 2K,48-PIN (OR MS7132)		R	11	1.000	EA	U13	Yes		

Assembly	Description	Group	PFC	Commodity	Class	Planner	Buyer	Drawing	Rev	LT
100773-0000	PCBA, 200MHZ DIGITAL SUBC., E2 REV. '01'(D055)				A				01	0

Shrinkage Factor: 0.000

ITEM	LEVEL	SEQ.	DESCRIPTION	REV	CL	LT	QUANTITY	U/M	REFERENCE	MLT	BEGIN	END
364000-0098A	*1	25	IC, 82C54,CTC		R	11	3.000	EA	U7,9,11	Yes		
364000-0102A	*1	26	IC, 27C512, EPROM, 200NS		R	11	1.000	EA	U8	Yes		
364000-0116A	*1	27	IC, LM337LZ,VOLT. REGULAT OR,TO-92 CASE		R	22	1.000	EA	U20	Yes		
364000-0117A	*1	28	IC, 5614 FILTER		R	22	4.000	EA	U1,23,3,25	Yes		
364000-0118A	*1	29	IC, 5615 FILTER		R	22	2.000	EA	U2,24	Yes		
364000-0119A	*1	30	IC, PAL, EP600 (AFTER PR OGRAMMING LABELED 4INTS)		R	22	1.000	EA	U12	Yes		
364000-0120A	*1	31	IC, 74HC259		R	22	1.000	EA	U14	Yes		
364000-0121A	*1	32	IC, 74HC11		R	22	1.000	EA	U16	Yes		
364000-0122A	*1	33	IC, 74HC132		R	22	1.000	EA	U18	Yes		
365000-0008A	*1	34	SKT, 8-POS,DIP,TIN PLATE, L.P.		R	11	8.000	EA	U1,2,3,21,23,24,25,26	Yes		
365000-0224A	*1	35	SOCKET, 24 PIN DIP		R	22	1.000	EA	U12	Yes		
365000-0014A	*1	36	SKT, 14-POS,DIP,TIN PLATE ,L.P.		R	11	7.000	EA	U4,5,15,16,17,18,19	Yes		
365000-0016A	*1	37	SKT, 16-POS,DIP,TIN PLATE ,L.P.		R	11	2.000	EA	U10,14	Yes		
365000-0024A	*1	38	SKT, 24-POS,DIP,TIN PLATE ,L.P.		R	11	3.000	EA	U7,9,11	Yes		
365000-0028A	*1	39	SKT, 28-POS,DIP,TIN PLATE ,L.P.		R	11	1.000	EA	U8	Yes		
365000-0040A	*1	40	SKT, 40-POS,DIP,TIN PLATE ,L.P.		R	11	1.000	EA	U6	Yes		
370100-0103A	*1	41	RES, 10K,1/4W,5%,CF		R	11	6.000	EA	R1,33,34,9,48,49	Yes		
370100-0104A	*1	42	RES, 100K,1/4W,5%,CF		R	11	6.000	EA	R37,39,40,38,24,25,	Yes		
370100-0104A	*1	43	RES, 100K,1/4W,5%,CF		R	11	2.000	EA	R2,12	Yes		
370100-0123A	*1	44	RES, 12K,1/4W,5%,CF		R	11	2.000	EA	R10,11	Yes		
370100-0154A	*1	45	RES, 150K,1/4W,5%,CF		R	11	2.000	EA	R14,16	Yes		
370100-0203A	*1	46	RES, 20K,1/4W,5%,CF		R	11	3.000	EA	R20,22,28	Yes		
370100-0204A	*1	47	RES, 200K,1/4W,5%,CF		R	11	2.000	EA	R41,42	Yes		
370100-0223A	*1	48	RES, 22K,1/4W,5%,CF		R	11	2.000	EA	R35,31	Yes		

Assembly	Description	Group	PFC	Commodity	Class	Planner	Buyer	Drawing	Rev	LT
400773-0000	PCBA, 200MHZ DIGITAL SUBC., E2 REV. '01'(D055)				A				01	0

Shrinkage Factor: 0.000

ITEM	LEVEL	SEQ.	DESCRIPTION	REV	CL	LT	QUANTITY	U/M	REFERENCE	MLT	BEGIN	END
370100-0302A	*1	49	RES, 3K,1/4W,5%,CF		R	11	2.000	EA	R13,17	Yes		
370100-0303A	*1	50	RES, 30K,1/4W,5%,CF		R	11	1.000	EA	R15	Yes		
370100-0472A	*1	51	RES, 4.7K,1/4W,5%,CF		R	11	4.000	EA	R43,19,23,29	Yes		
370100-0473A	*1	52	RES, 47K,1/4W,5%,CF		R	11	3.000	EA	R26,36,30	Yes		
370100-0474A	*1	53	RES, 470K,1/4W,5%,CF		R	11	3.000	EA	R18,21,27	Yes		
370100-0512A	*1	54	RES, 5.1K,1/4W,5%,CF		R	11	3.000	EA	R3,4,5	Yes		
370100-0684A	*1	55	RES, 680K,1/4W,5%,CF		R	11	3.000	EA	R6,7,8	Yes		
370200-1001A	*1	56	RES, 1K,1/4W,1%,MF		R	11	2.000	EA	R45,47	Yes		
370200-1500A	*1	57	RES, 150,1/4W,1%,MF		R	11	2.000	EA	R44,46	Yes		
376000-0003A	*1	58	XSTR, 2N3904		R	11	3.000	EA	Q3,4,6	Yes		
376000-0011A	*1	59	XSTR, 2N3906,SIGNAL		R	11	2.000	EA	Q5,9	Yes		
376000-0019A	*1	60	XSTR, 2N7000,FET		R	11	2.000	EA	Q7,10	Yes		
376000-0020A	*1	61	XSTR, J201,FET		R	11	3.000	EA	Q1,2,8	Yes		
400772-0000	*1	62	PCB, DIGITAL SUBCARRIER, REVISION 'E'		R	33	1.000	EA		Yes		
360500-0048A	*1	63	SPCR, 1/4 X 1/4,SWAGE TYP E		R	11	1.000	EA		Yes		
364000-0129A	*1	65	IC, ADC0831CCN		R	22	1.000	EA	U26	Yes		
365000-0148A	*1	66	SOCKET, 48 PIN DIP		R	22	1.000	EA	U13	Yes		

Cumulative Lead Time for 400773-0000 = 77

Assembly	Description	Group	PFC	Commodity Class	Planner	Buyer	Drawing	Rev	LT
400919-0000	PCBA, 450MHZ LR DIG.SUBC., REVISION "C" - E2/E4			A				C	0

Shrinkage Factor: 0.000

ITEM	LEVEL	SEQ.	DESCRIPTION	REV	CL	LT	QUANTITY	U/M	REFERENCE	MLT	BEGIN	END
400773-0000	*1	1	PCBA, 200MHZ DIGITAL SUBC ., E2 REV. '01'(D055)	01	A	0	1.000	EA	W/FOLLOWING REVISIONS	Yes		
364000-0117A	*1	2	IC, 5614 FILTER		R	22	-2.000	EA	REMOVE U1 AND U23	Yes		
364000-0118A	*1	3	IC, 5615 FILTER		R	22	2.000	EA	U1, U23 ISS THIS ONLY	Yes		

Cumulative Lead Time for 400919-0000 = 22

SWITCHING POWER SUPPLY BOARD

CHAPTER 6

6.0.0 SWITCHING POWER SUPPLY BOARD

6.1.0 INPUT CIRCUITRY

The **ESCORT 400** series monitor is powered by one type of input, a standard AC 110 - voltage. The AC line voltage enters the switching power supply at the 3 pin connector (P-1) and passes through the power transformer where the line voltage is stepped down to approximately 40 volts AC. Common mode filtering is done by L1, C20, C21, C1 and C2. CR1 provides full wave rectification. The LCR circuit consisting of C3, C4, R1, R31 and L2 eliminate the DC ripple and form a differential filter. This filters the high frequency noise created from T1 and T2. With the ON/STANDBY switch in the "ON" position Q1 initializes the pulse width modulator, U1, until 15VDC is produced by the power supply and fed back through D20. D20 will turn off Q1. This allows the power supply to run off its own DC output, therefore increasing its efficiency. Q2 is used as a current limiter for overload protection.

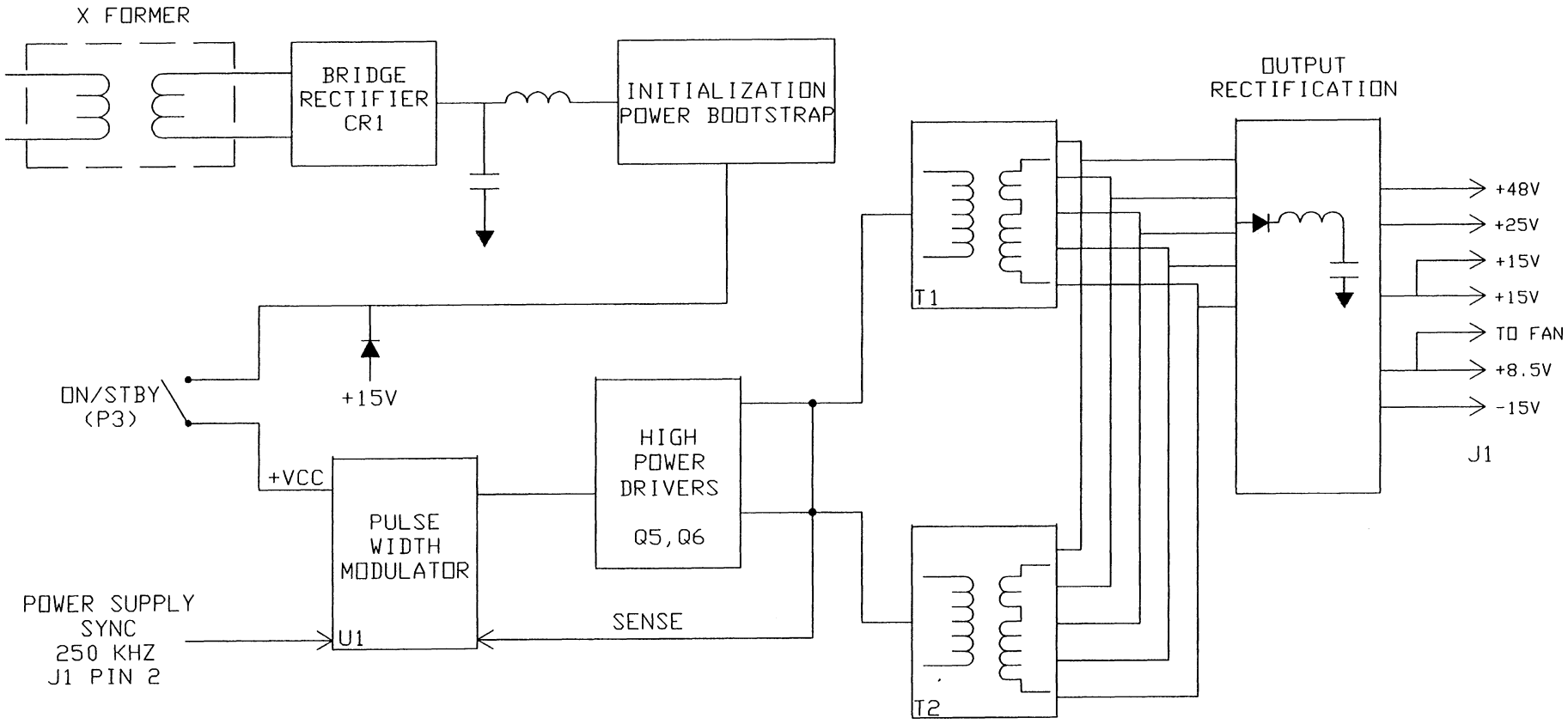
6.2.0 SYNCHRONIZATION AND SENSE CIRCUITS

The Power Supply Sync signal (PS SYNC) coming in from the CPU, at (J1-2), is a 250KHz pulse signal passing through Q3 and locking into the reference oscillator, C11, thus synchronizing the pulse width modulator at U1 pin 8. This is used to improve noise immunity in the system at U1 pin 2 an internal 5V reference for Q3, Q4 and is used to set the maximum current limit of the supply at pin 1.

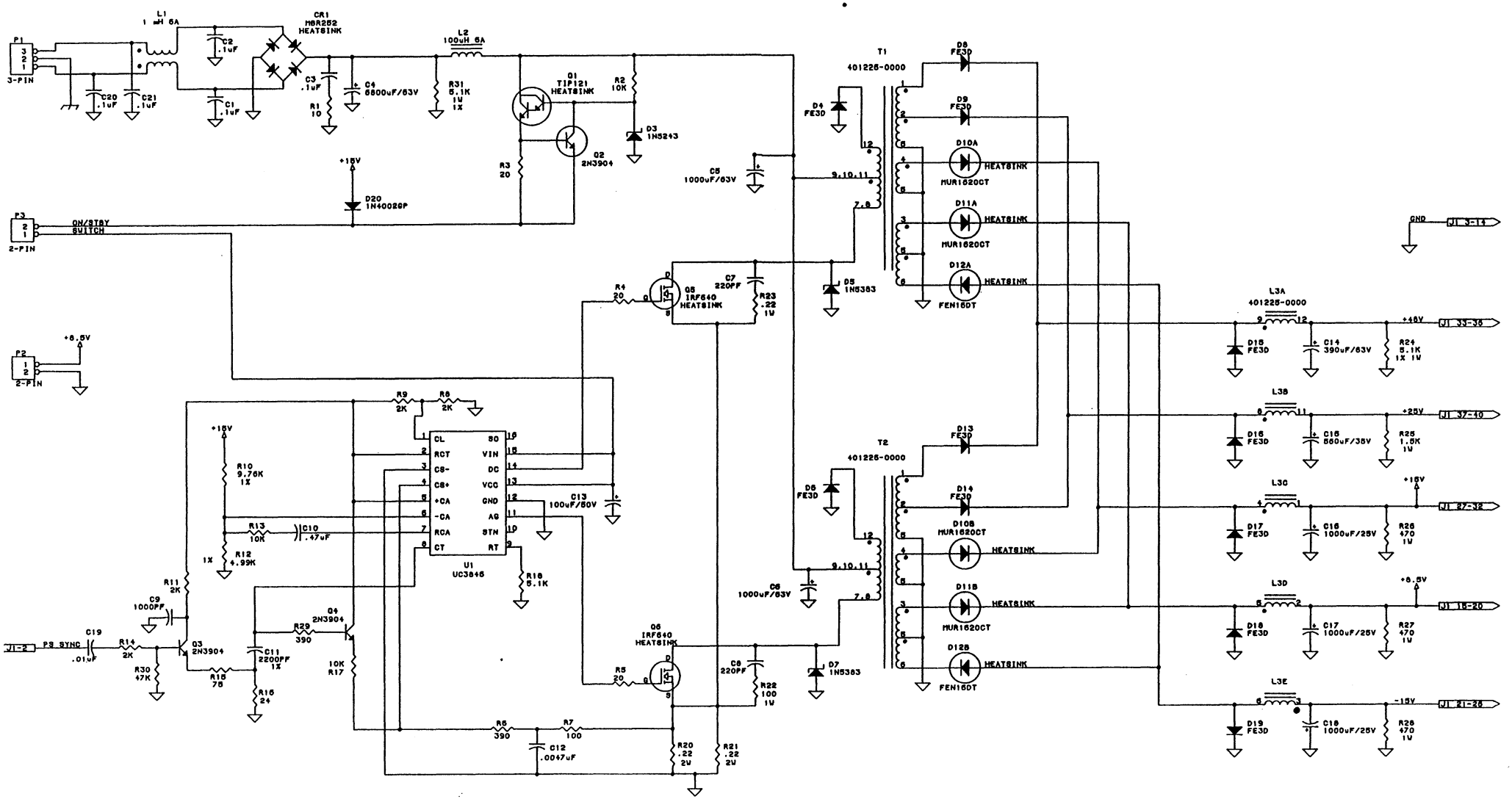
Current sense is looped back to U1 pin 4 from the source of Q5 and Q6, through a filter formed by R6, R7 and C12. Q4 is used as a slope compensator for the current sense. The voltage sense comes in to U1 pin 6. These two sense signals are used to stabilize the outputs of the pulse width modulator (U1).

6.3.0 DC OUTPUT VOLTAGES

When U1 is initialized by the ON/STANDBY switch, the pulse width modulator generates a pulse waveform at pins 11, 14. This waveform switches Q5 and Q6 out of phase with one another, and drives the transformers T1 and T2. The secondary AC voltages are then rectified by D8, D9, D11A, D12A, D13, D14, D10B, D11B, D12B. The pulsating DC is filtered by its respective L, C network to produce constant DC output voltages. R24 through R28 are bleed resistors for the filter caps C14 to C18. There are five DC output voltages from the supply; they are +48V, +25V, +15V, -15V and +8.5V all going out the J-1 connector. 8.5V also is being supplied to the 2 pin connector (P2) which is used to power the fan.



SWITCHING POWER SUPPLY BOARD BLOCK DIAGRAM

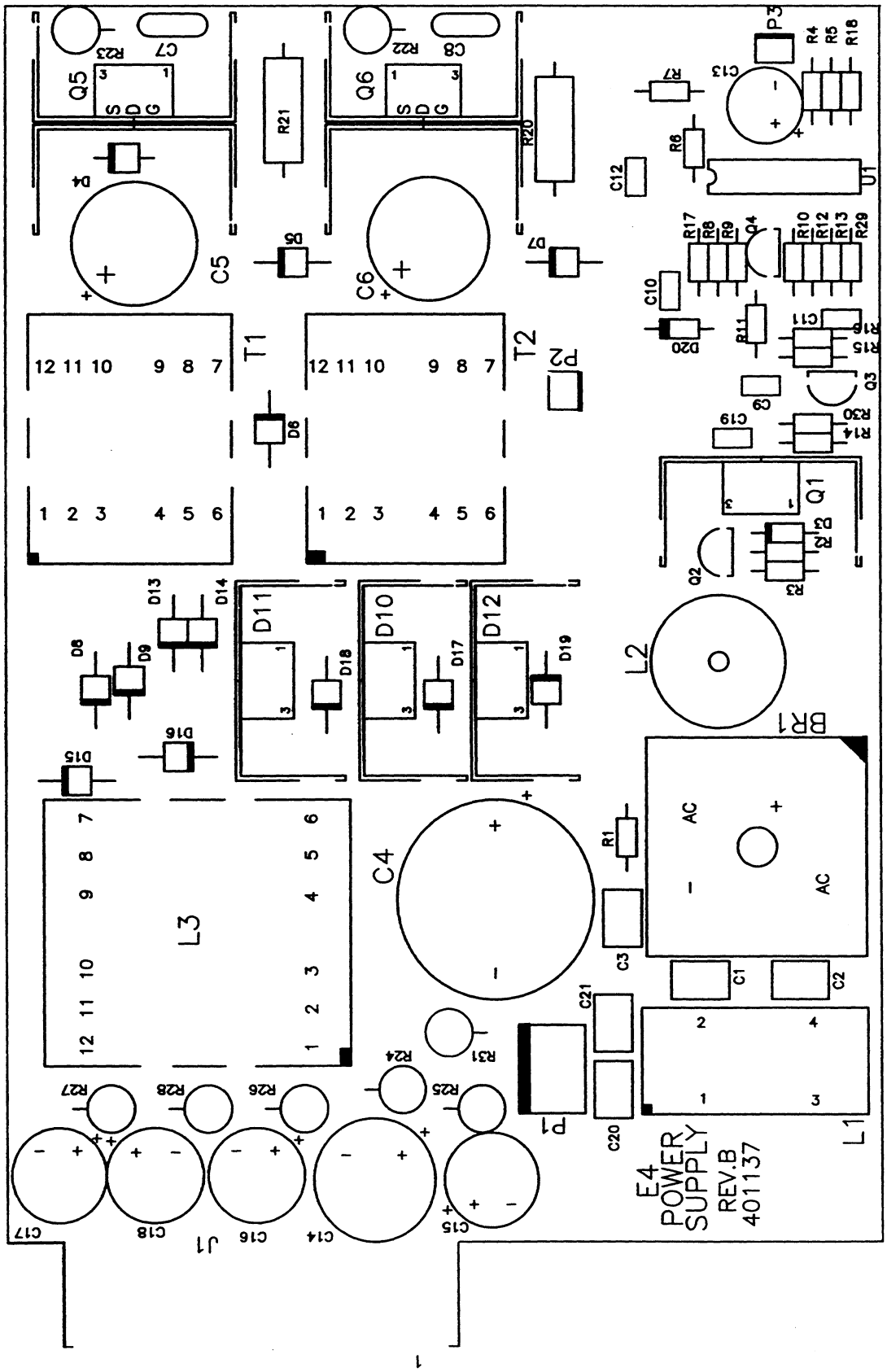


6-3

1. RESISTORS ARE 1/4W 5% CF

FILENAME = E4PS.SCH

MEDICAL DATA ELECTRONICS		
Title: E4 POWER SUPPLY		
Size: C	Document Number: 401138	REV: A


E4
POWER
SUPPLY
REV.B
401137
T1
T2
L1
L2
L3
BR1
C4
C5
C6
P1
P2
P3
Q1
Q2
Q3
Q4
Q5
Q6
U1
J1

ssembly	Description	Group	PFC	Commodity Class	Planner Buyer	Drawing	Rev	LT
01138-0000	PCBA, POWER SUPPLY E4 REV. A			A				5

hrinkage Factor: 0.000

ITEM	LEVEL	SEQ.	DESCRIPTION	REV	CL	LT	QUANTITY	U/M	REFERENCE	MLT	BEGIN	END
401137-0000	*1	1	PCB, POWER SUPPLY E4 REV. B	B	R	33	1.000	EA	PC1	Yes		
370100-0100A	*1	2	RES, 10,1/4W,5%,CF		R	11	1.000	EA	R1	Yes		
370100-0103A	*1	3	RES, 10K,1/4W,5%,CF		R	11	3.000	EA	R2,13,17	Yes		
370100-0200A	*1	4	RES, 20,1/4W,5%,CF		R	11	3.000	EA	R3,4,5	Yes		
370100-0101A	*1	5	RES, 100,1/4W,5%,CF		R	11	1.000	EA	R7	Yes		
370100-0391A	*1	6	RES, 390,1/4W,5%,CF		R	11	2.000	EA	R6,29	Yes		
370100-0202A	*1	7	RES, 2K,1/4W,5%,CF		R	11	4.000	EA	R8,9,11,14	Yes		
370200-4991A	*1	8	RES, 4.99K,1/4W,1%,MF		R	11	1.000	EA	R12	Yes		
370100-0750A	*1	9	RES, 75,1/4W,5%,CF		R	11	1.000	EA	R15	Yes		
370100-0240A	*1	10	RES, 24,1/4W,5%,CF		R	11	1.000	EA	R16	Yes		
370203-2200A	*1	11	RES, 0.22,2W,5%,M.O.		R	22	2.000	EA	R20,21	Yes		
370201-0101A	*1	12	RES, 100,1W,METAL OXIDE		R	11	2.000	EA	R22,23	Yes		
370100-0512A	*1	13	RES, 5.1K,1/4W,5%,CF		R	11	1.000	EA	R18	Yes		
370201-0512A	*1	14	RES, 5.1K,1W,1%,METAL OXIDE		R	11	2.000	EA	R24,31	Yes		
370201-0152A	*1	15	RES, 1.5K,1W,5%		R	22	1.000	EA	R25	Yes		
370201-0471A	*1	16	RES, 470,1W,5%		R	33	3.000	EA	R26,27,28	Yes		
370200-9761A	*1	17	RES, 9.76K,1/4W,1%,MF		R	11	1.000	EA	R10	Yes		
370100-0473A	*1	18	RES, 47K,1/4W,5%,CF		R	11	1.000	EA	R30	Yes		
360600-0037A	*1	19	HTSNK, E4 SWITCHING P.S.		R	33	9.000	EA	HS1-HS9	Yes		
352302-0104A	*1	20	CAP, 0.1uF,100V,20%,RAD,MYLAR		R	22	5.000	EA	C1,2,3,20,21	Yes		
352201-0688A	*1	21	CAP, 6800UF,63V, RAD, ELECT (+80-20%) 25MM X 50MM		R	33	1.000	EA	C4	Yes		
352200-0108A	*1	22	CAP, 1000uF,63V,RAD,ELECT		R	22	2.000	EA	C5,6	Yes		
352102-0221A	*1	23	CAP, 220pF,20%,1kV,CER,DISC		R	22	2.000	EA	C7,8	Yes		
352300-0102A	*1	24	CAP, 1000PF,50V,20%,RAD,MYLAR		R	22	1.000	EA	C9	Yes		

Assembly	Description	Group	PFC	Commodity Class	Planner	Buyer	Drawing	Rev	LT
401138-0000	PCBA, POWER SUPPLY E4 REV. A			A					5

Shrinkage Factor: 0.000

ITEM	LEVEL	SEQ.	DESCRIPTION	REV	CL	LT	QUANTITY	U/M	REFERENCE	MLT	BEGIN	END
352300-0474A	*1	25	CAP, .47UF, 50V,20%,RAD,MYLAR(METALLIZED POLYESTR)		R	22	1.000	EA	C10	Yes		
352300-0222A	*1	26	CAP, 2200PF,50V OR 100V,1%,MYLAR,.15L.S.		R	77	1.000	EA	C11	Yes		
352300-0472A	*1	27	CAP, .0047UF,50V,20%,MYLAR		R	22	1.000	EA	C12	Yes		
352200-0107A	*1	28	CAP, 100UF,50V,RAD,ELECT, LS TYPE		R	22	1.000	EA	C13	Yes		
352200-0397A	*1	29	CAP, 390uF,63V,LOW ESR,ELECT (16 x 20mm)		R	33	1.000	EA	C14	Yes		
352200-0567A	*1	30	CAP, 560uF,35V,LOW ESR,ELECT (12.5 x 20mm)		R	33	1.000	EA	C15	Yes		
352201-0108A	*1	31	CAP, 1000uF,25V,LOW ESR,ELECT (12.5 x 25mm)		R	66	3.000	EA	C16,17,18	Yes		
352300-0103A	*1	32	CAP, .01UF,50V,20%,RAD,MYLAR		R	22	1.000	EA	C19	Yes		
378000-0031A	*1	33	DIO, FE3D,200V,3A,ULTRAFAST-2ND OP PREP ARGOSY		R	11	8.000	EA	D4,6,8,9,13,14,15,16	Yes		
378000-0031A	*1	34	DIO, FE3D,200V,3A,ULTRAFAST-2ND OP PREP ARGOSY		R	11	3.000	EA	D17,18,19	Yes		
378000-0050A	*1	35	DIO, 1N5383,5W,150V,ZENER **MOT ONLY**		R	33	2.000	EA	D5,7	Yes		
378000-0002A	*1	36	DIO, 1N4002GP,RCTFR, (MOT ONLY) T&R		R	11	1.000	EA	D20	Yes		
378000-0033A	*1	37	DIO, MUR1620CT,200V,16A,RCTFR,ULTRAFAST,COM ANOD		R	11	2.000	EA	D10,11	Yes		
378000-0032A	*1	38	DIO, FEN16DT,150V,16A,RCTFR,ULTRAFAST,COM ANOD		R	22	1.000	EA	D12	Yes		
376000-0009A	*1	39	XSTR, TIP121,DARLINGTON PWR		R	11	1.000	EA	Q1	Yes		
376000-0003A	*1	40	XSTR, 2N3904		R	11	3.000	EA	Q2,3,4	Yes		
376000-0025A	*1	41	XSTR, IRF640,200V,18A,MOSFET (TO 220 PKG)		R	33	2.000	EA	Q5,6	Yes		
364000-0165A	*1	42	IC, UC3846,CURRENT MODE PWM CONTROLLER		R	33	1.000	EA	U1	Yes		
382200-0025A	*1	43	CHOKE, 1mH,6 AMP,COMMON MODE		R	33	1.000	EA	L1	Yes		
382200-0026A	*1	44	CHOKE, 100uH,6 AMP,POWER		R	33	1.000	EA	L2	Yes		
401225-0000	*1	45	MULTI-INDUCTOR E4 PWR SPPLY REV. A		R	33	1.000	EA	L3	Yes		
401226-0000	*1	46	XFMR, FERRITE E4 PWR SPPLY REV. A		R	33	2.000	EA	T1,2	Yes		
378000-0048A	*1	47	DIO, 25A,200V,BRIDGE RECTFR		R	33	1.000	EA	BR1	Yes		
378000-0049A	*1	48	DIO, 1N5243A,13V,500MW,ZENER **MOT ONLY**		R	33	1.000	EA	D3	Yes		

sembly	Description	Group	PFC	Commodity Class	Planner Buyer	Drawing	Rev	LT
)1138-0000	PCBA, POWER SUPPLY E4 REV. A			A				5

rinkage Factor: 0.000

ITEM	LEVEL	SEQ.	DESCRIPTION	REV	CL	LT	QUANTITY	U/M	REFERENCE	MLT	BEGIN	END
358100-0013A	*1	49	SCR, 4-40 X 3/8,PH PNHD,CAD1		R	11	6.000	EA	1 - DO NOT ISSUE	Yes		
358100-0022A	*1	50	SCR, 4-40 X 3/4,PH PNHD		R	11	1.000	EA	2 - DO NOT ISSUE	Yes		
358200-0001A	*1	51	WSHR, SHLDR		R	11	6.000	EA	3 - DO NOT ISSUE	Yes		
358200-0009A	*1	52	WSHR, #4 SPLIT LOCK		R	11	7.000	EA	4 - DO NOT ISSUE	Yes		
360500-0022A	*1	53	NUT, #4 HEX,LRG PTTRN		R	11	7.000	EA	5 - DO NOT ISSUE	Yes		
358200-0004A	*1	54	WSHR, #4 FLAT STL CAD1,(.125ID,9/32OD,.025THK)		R	11	12.000	EA	6 - DO NOT ISSUE	Yes		
360500-0040A	*1	55	HARDWARE, ISO-THERM PAD, TO-220		R	11	6.000	EA	7 - DO NOT ISSUE	Yes		
354000-0085A	*1	56	CONN, 3-PIN,M,STRT LCK,.156 CTR		R	11	1.000	EA	P1	Yes		
354000-0138A	*1	57	CONN, 2-P,M,STRT LOCK,.1 CTR,HDR		R	11	2.000	EA	P2, P3	Yes		
360500-0005A	*1	58	STDOFF, 4-40 X 1/4,1/16,SWAGE TYPE		R	11	2.000	EA		Yes		
365000-0016A	*1	59	SKT, 16-POS,DIP,TIN PLATE ,L.P.		R	11	1.000	EA		Yes		

Cumulative Lead Time for 401138-0000 = 82

MECHANICAL DISASSEMBLY

CHAPTER 7

7.0.0 MECHANICAL DISASSEMBLY

CAUTION:

Only qualified technicians should attempt to perform repairs or removal of any parts in the **ESCORT 400**. Opening the **ESCORT 400** could violate warranty.

Read all Disassembly Instructions prior to performing any removal of parts.

Refer to the Connector Placement drawing when replacing connectors.

7.1.0 SAFETY

High voltage is exposed when the covers are removed from the monitor. Disconnect the AC power cord to insure that current is removed from the unit. Always observe safe working techniques when troubleshooting or removing components. Work surfaces should be free of any stray metal parts.

The components in the **ESCORT** monitor are static sensitive. Use an electro-static discharge kit whenever handling printed circuit boards.

7.2.0 FUSE REPLACEMENT

There is a 2.0 amp slow blow fuse located in the power module at the rear panel. The module can be removed by prying the tab at the low center area of the module with a flat bladed screwdriver. Pull out the fuse holder and replace the fuse if needed.

7.3.0 REASSEMBLY

This chapter includes removal instructions only: The reinstallation of assemblies is opposite of removal.

7.4.0 DISASSEMBLY

7.4.1 TOP COVER

Remove the screws on each side of the monitor. Lift the chassis out of the bottom cover.

7.4.2 BOTTOM COVER

Remove the three screws on each side of the monitor, lift the chassis out of the bottom cover. Disconnect the 40 pin ribbon cable at J4 on the CPU card. Remove the four cables at the antenna module at inside, rear top of system.

CAUTION: When reassembling the unit, make sure all top and bottom screws are replaced. Failure to do so could cause the unit to come apart in transport.

7.4.3 BEZEL ASSEMBLY

Using a phillips head screwdriver, back out the two screws on both sides and top of front bezel. Remove lugged wires from ON/STANDBY switch. Disconnect flex cable from J1 on CPU. Back out the six nuts holding bezel to bezel frame. Separate bezel from frame.

7.4.4 RECORDER REMOVAL

Remove top and bottom covers. Open the door of the recorder and remove the roll of paper. Using a Phillips head screwdriver, back out the two screws on both sides and top of front bezel, Remove bezel. Back out the two screws that mount the recorder bracket to the CRT bracket. Pull out the recorder slightly, to allow some space to reach the connector on back of the recorder. Remove 34 pin cable from back of recorder. Remove power harness from recorder. Back out the two screws on the recorder bracket. Lift the recorder out of the chassis.

7.4.5 PROCESSOR BOARDS

Remove top and bottom covers. Back out the long screw on the rear panel above the heatsink. Pull screw out slowly, noting the spacers in between each board. Pull out spacers as screw is being removed. Processor boards can now be removed.

CAUTION:

Be very careful when replacing the processor boards. Be sure that all four cards are securely in the connector slots.

7.4.6 SWITCHING POWER SUPPLY

Remove top and bottom covers. Back out the two screws on mounting bracket, securing the power supply. Unplug connectors at P-2, P-3, and P-1. Pull upward, removing board from J-12 slot of CPU. Lift power supply out of the system.

CAUTION:

Be very careful when replacing the power supply back in J-12. Make sure the power supply is securely in its slot.

7.4.7 CPU REMOVAL

Remove top and bottom covers, processor boards, and switching power supply. Also, remove J-1 and J-2 from CPU board. Back out the four, number 6, 3/8" phillips head screws from the CPU. Back out the eight allen screws from rear panel heatsink assembly. Pull CPU out away from chassis, noting that J-3 of CPU is plugged into four channel daughter board. Be very careful pulling CPU back and forth slightly, working it slowly away from four channel daughter board.

7.4.8 CRT REMOVAL

Remove top and bottom covers. Back out the six screws holding in the bezel. There are two screws on each side of the panel and two underneath. **CAUTION:** Handle CRT with care, implosion can occur. Discharge CRT before removing. Take long bladed screwdriver and insert under rubber cover of anode on top of CRT. Make contact with anode of CRT and long screwdriver to metal chassis. Back out four screws holding in CRT. Remove Z-axis board away from rear of CRT. Remove J-11 from CPU. Pull CRT away from unit.

7.4.9 Z-AXIS BOARD

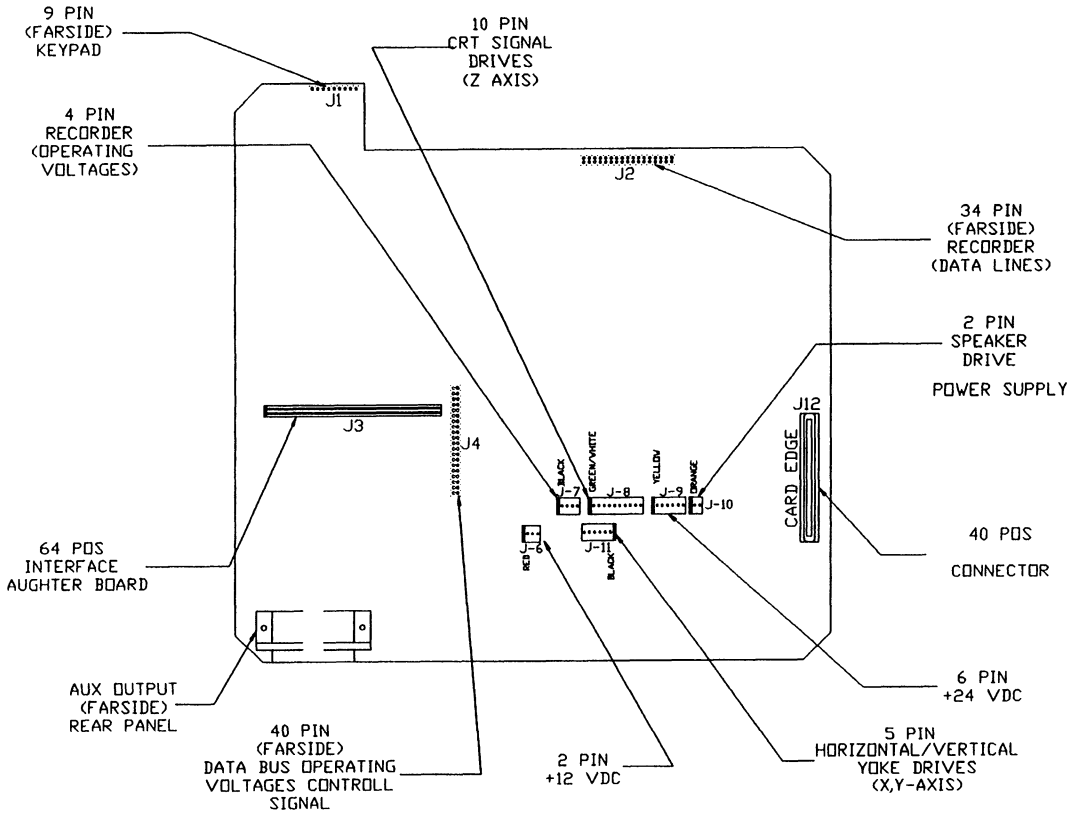
Remove top cover. Make sure AC plug is removed. Take a long bladed screwdriver and insert under rubber cover at anode of CRT. Make contact with chassis of system with screwdriver and slide screwdriver, touching anode of CRT, discharging it to the chassis of system. Remove Z-axis board from CRT filament. Remove connector from J8 on Z-axis board.

7.4.10 HIGH VOLTAGE POWER SUPPLY

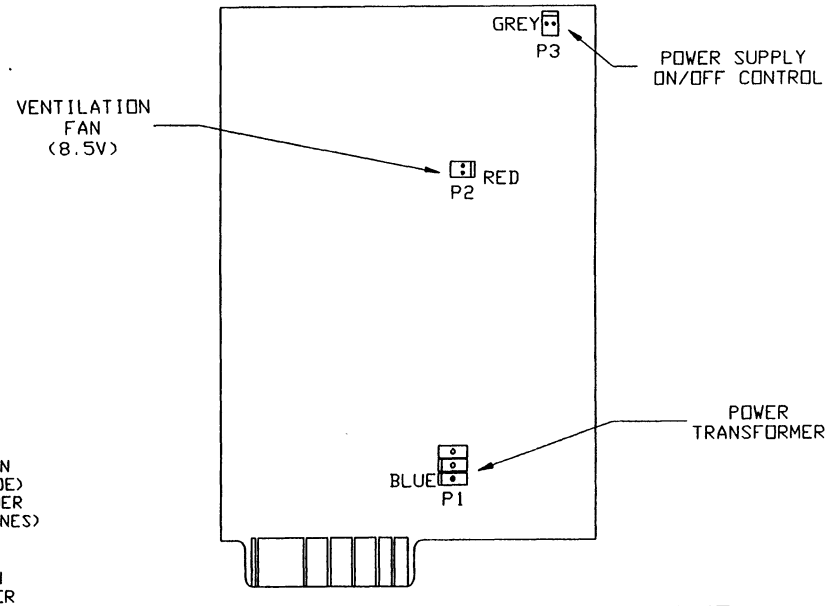
Remove top and bottom cover, bezel and CRT. Back out the two screws holding down the high voltage power supply. Remove J-9 from CPU. Take long bladed screwdriver and insert under rubber cover at anode of CRT. Make contact with chassis of system with screwdriver and slide screwdriver, touching anode of CRT discharging to the chassis of system. Pull high voltage power out of system.

7.4.11 TRANSFORMER

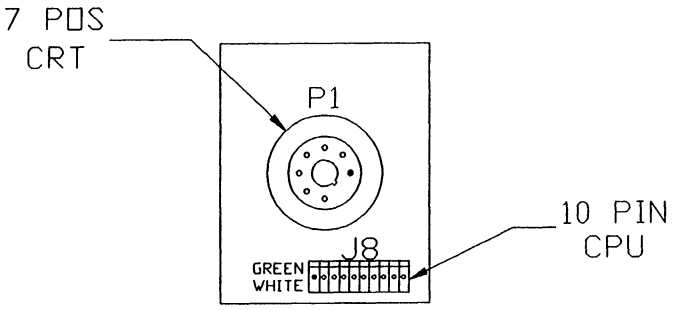
Remove AC fuse at rear of system, top and bottom covers and front bezel. Remove upper left hand CRT mounting screw. Cut tie-wraps holding AC wires at transformer module. Disconnect AC wires at power module. Back out two flat head screws on lower left hand side chassis bracket. Transformer, bracket and cover can now be pulled straight out forward front of system. Remove cover by backing out four pan head screws (two on each side of module). Remove remaining four flat head screws for complete removal of transformer.



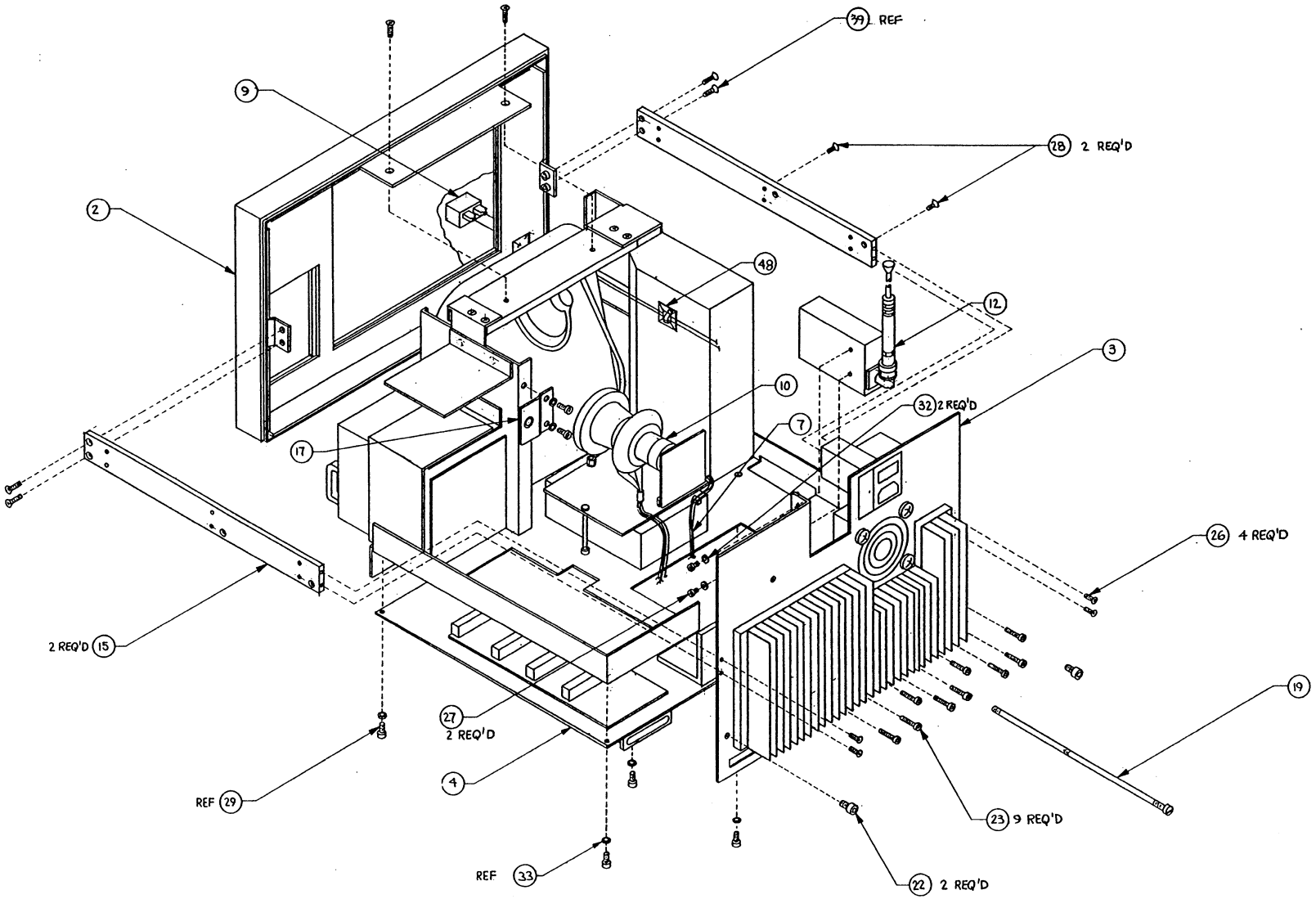
CPU CONNECTOR PLACEMENT



POWER SUPPLY CONNECTOR PLACEMENT



Z-AXIS CONNECTOR PLACEMENT



REVISIONS

LTR	DESCRIPTION	DATE	APPROVED

REV: B

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
X X °

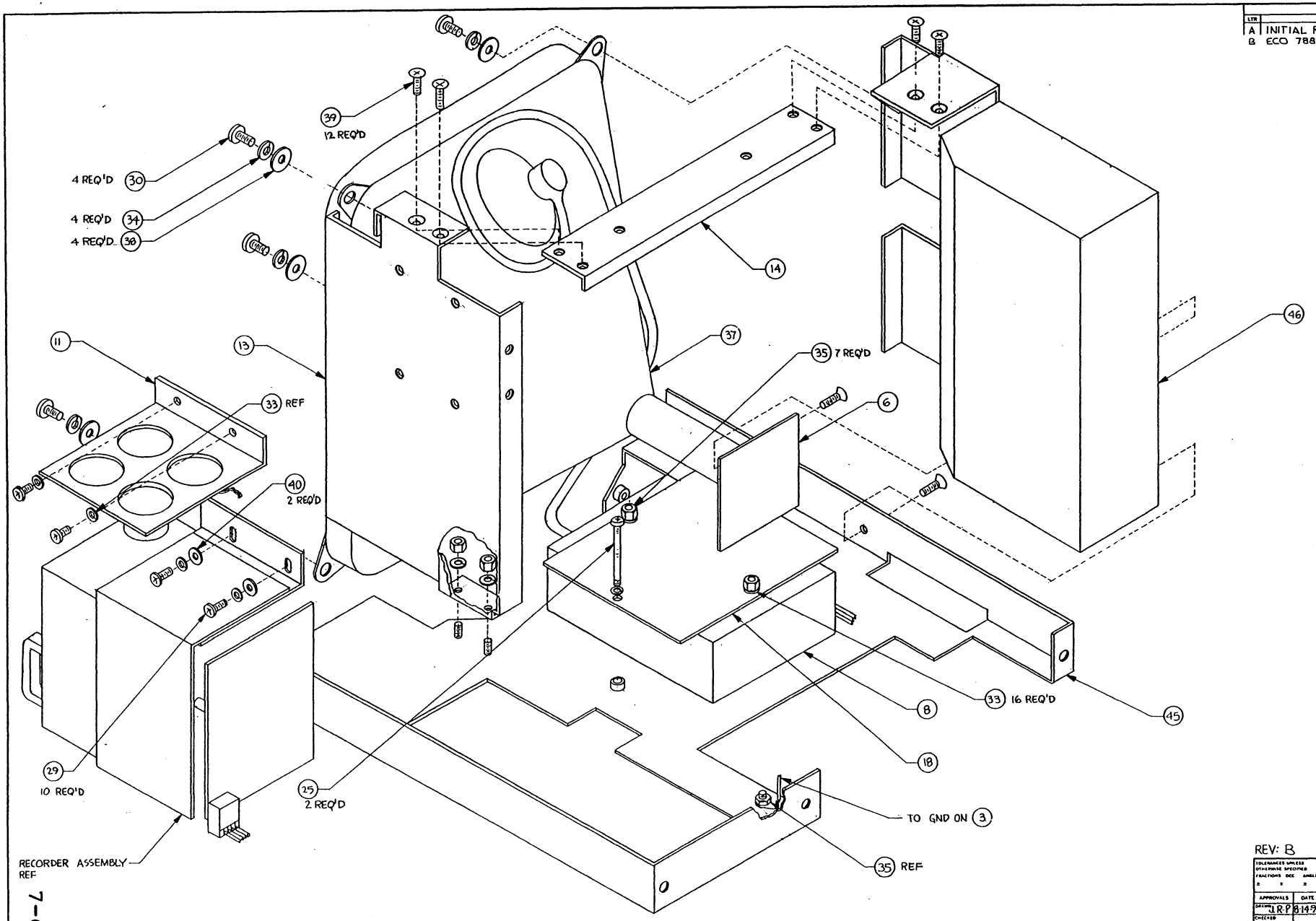
APPROVALS	DATE
DRAWN	
CHECKED	

MEDICAL DATA ELECTRONICS

CHASSIS ASSEMBLY E4

SCALE 1/2 | SIZE D | DRAWING NO. 500116

DO NOT SCALE DRAWING | SHEET 2 OF 3



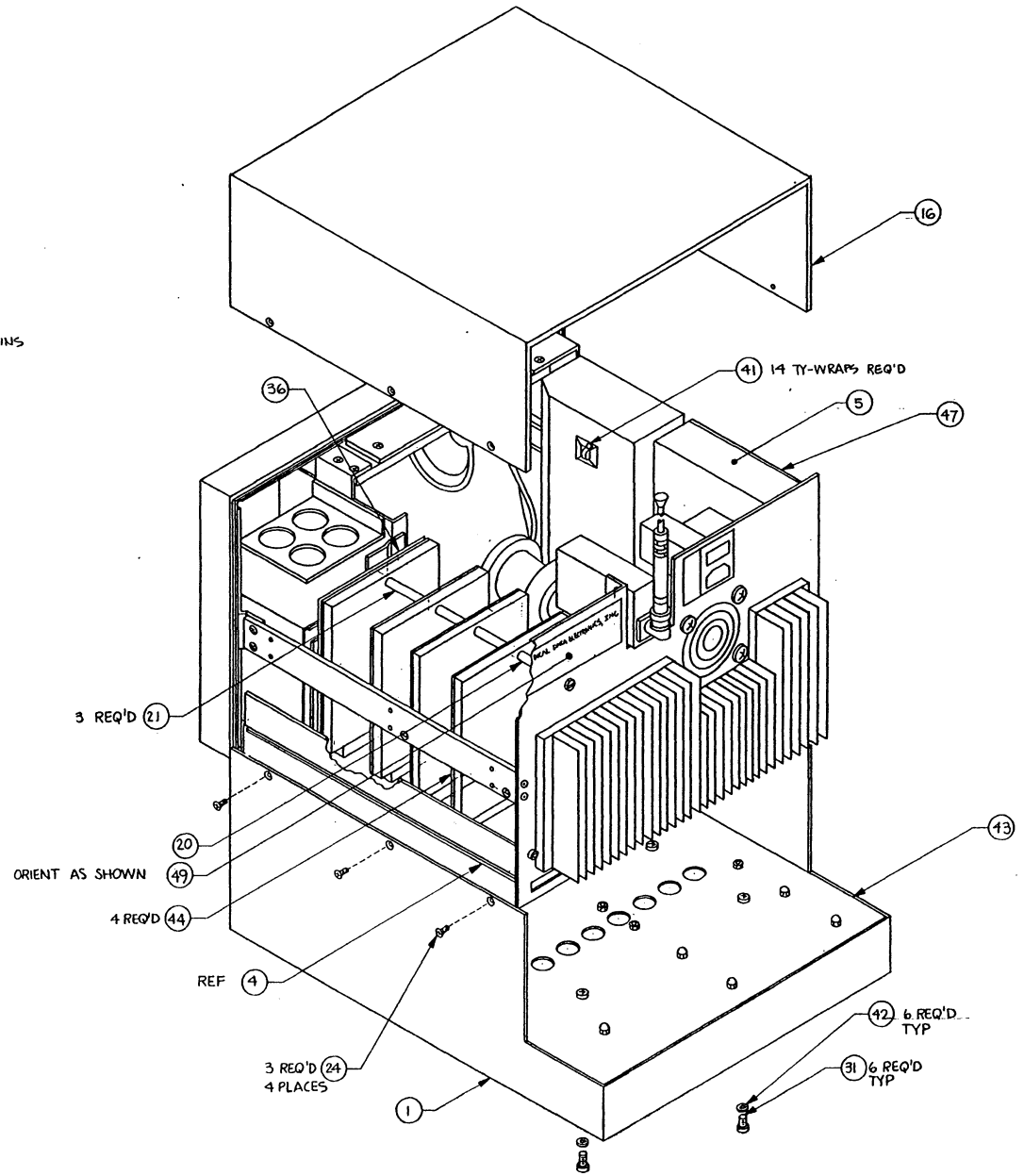
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE		
B	ECO 788	10-24-70	

REV: B

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ±	MDE	MEDICAL DATA ELECTRONICS
APPROVALS	DATE	CHASSIS ASSEMBLY E4
DRAWN LRP	8-14-70	
CHECKED		SCALE FULL · SIZE D · DRAWING NO. 500116
		DO NOT SCALE DRAWING · SHEET 1 OF 3

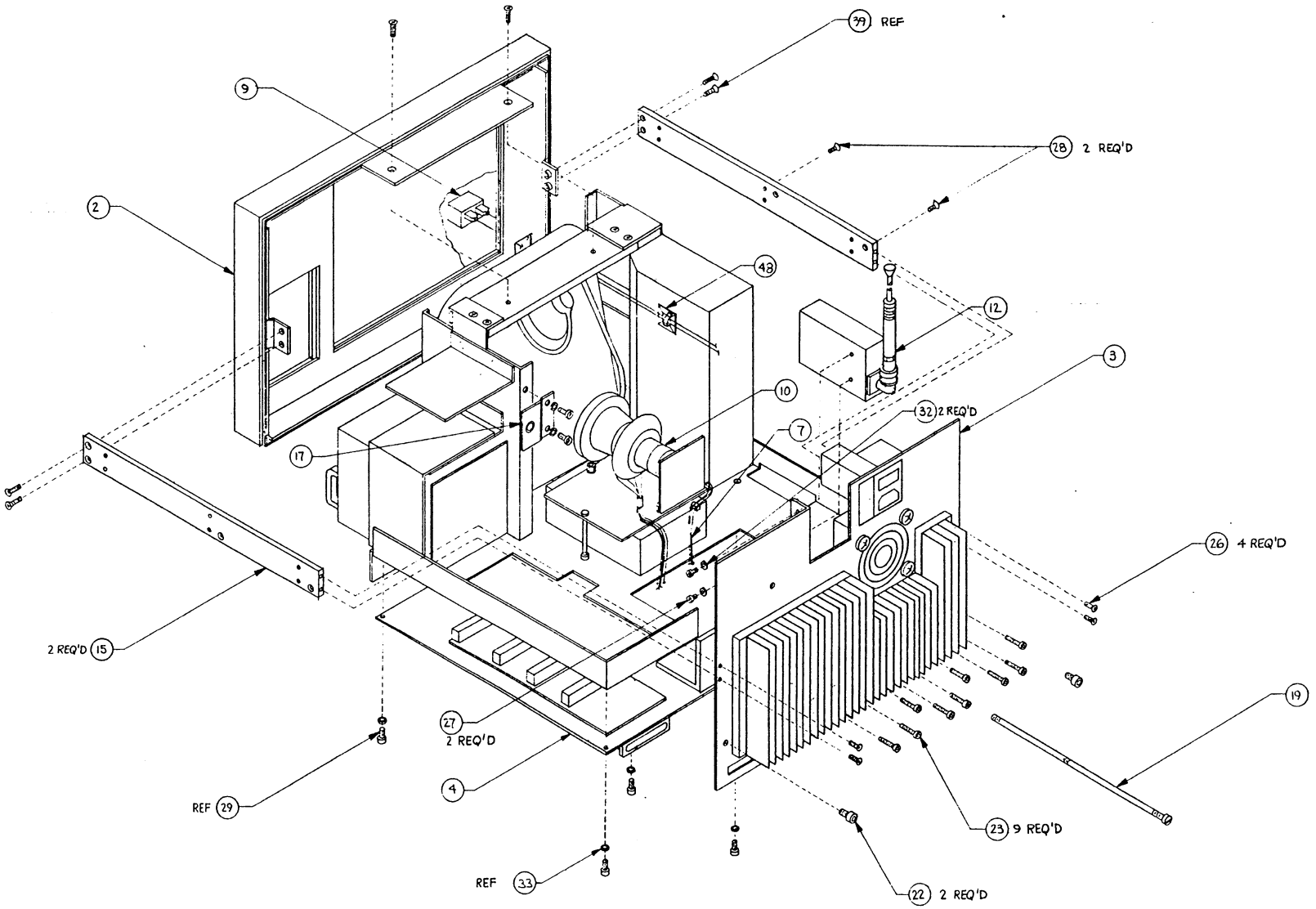
NOTES: UNLESS OTHERWISE SPECIFIED
CABLE/HARNESS CONNECTIONS

1. CPU J1 TO BEZEL
2. CPU J2 TO UPPER RECORDER
3. CPU J3 TO CPU INTERFACE
4. CPU J4 TO RECEIVERS
5. CPU J5 TO REAR PANEL
6. CPU J6 TO SPLITTER ASSY
7. CPU J7 TO LOWER RECORDER
8. CPU J8 TO Z-AXIS PCBA J8
9. CPU J9 TO HVPS
10. CPU J10 TO SPEAKER
11. CPU J11 TO YOKE
12. CPU J12 TO POWER SUPPLY J1
13. P.S. P1 TO TRANSFORMER 3PIN CONN.
14. P.S. P2 TO FAN, REAR PANEL
15. P.S. P3 TO BEZEL SWITCH
16. P.S. J1 TO CPU J12
17. RECEIVER 4 CONNECTORS TO SPLITTER ASSY 8 PINS
18. INTERFACE J1 TO DIGITAL SUBCARRIER
19. INTERFACE J2 TO DIGITAL SUBCARRIER
20. INTERFACE J3 TO DIGITAL SUBCARRIER
21. INTERFACE J4 TO DIGITAL SUBCARRIER
22. Z-AXIS P1 TO CRT



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES	MEDICAL DATA ELECTRONICS	
APPROVALS DATE	CHASSIS ASSEMBLY E4	
DRAWN		
CHECKED	SCALE 1/2	SIZE D DRAWING NO. 500116
	DO NOT SCALE DRAWING	SHEET 3 OF 3



REVISIONS

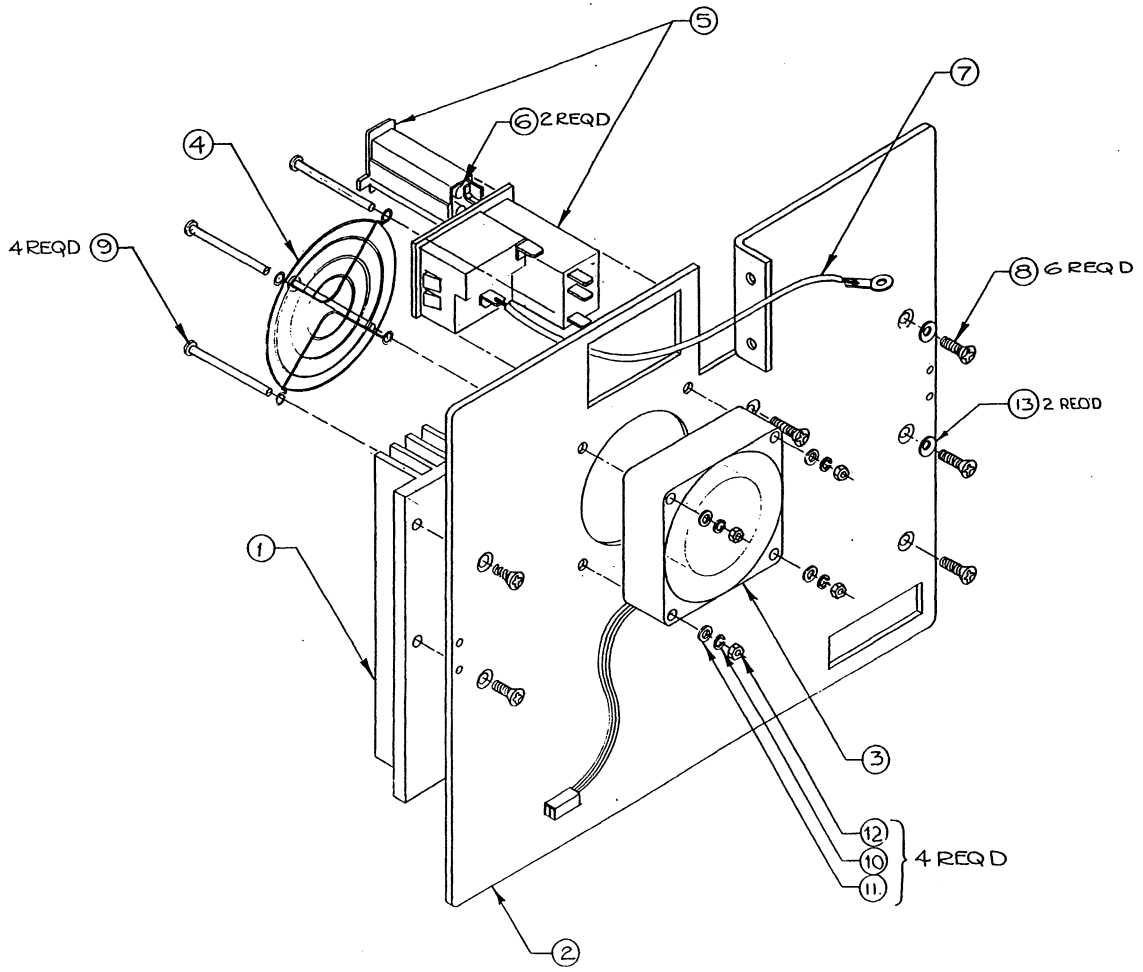
LTR	DESCRIPTION	DATE	APPROVED

REV: B

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES		MEDICAL DATA ELECTRONICS
APPROVALS	DATE	CHASSIS ASSEMBLY E4
DRAWN		
CHECKED		SCALE 1/2 SIZE D DRAWING NO 500116
		DO NOT SCALE DRAWING SHEET 2 OF 3

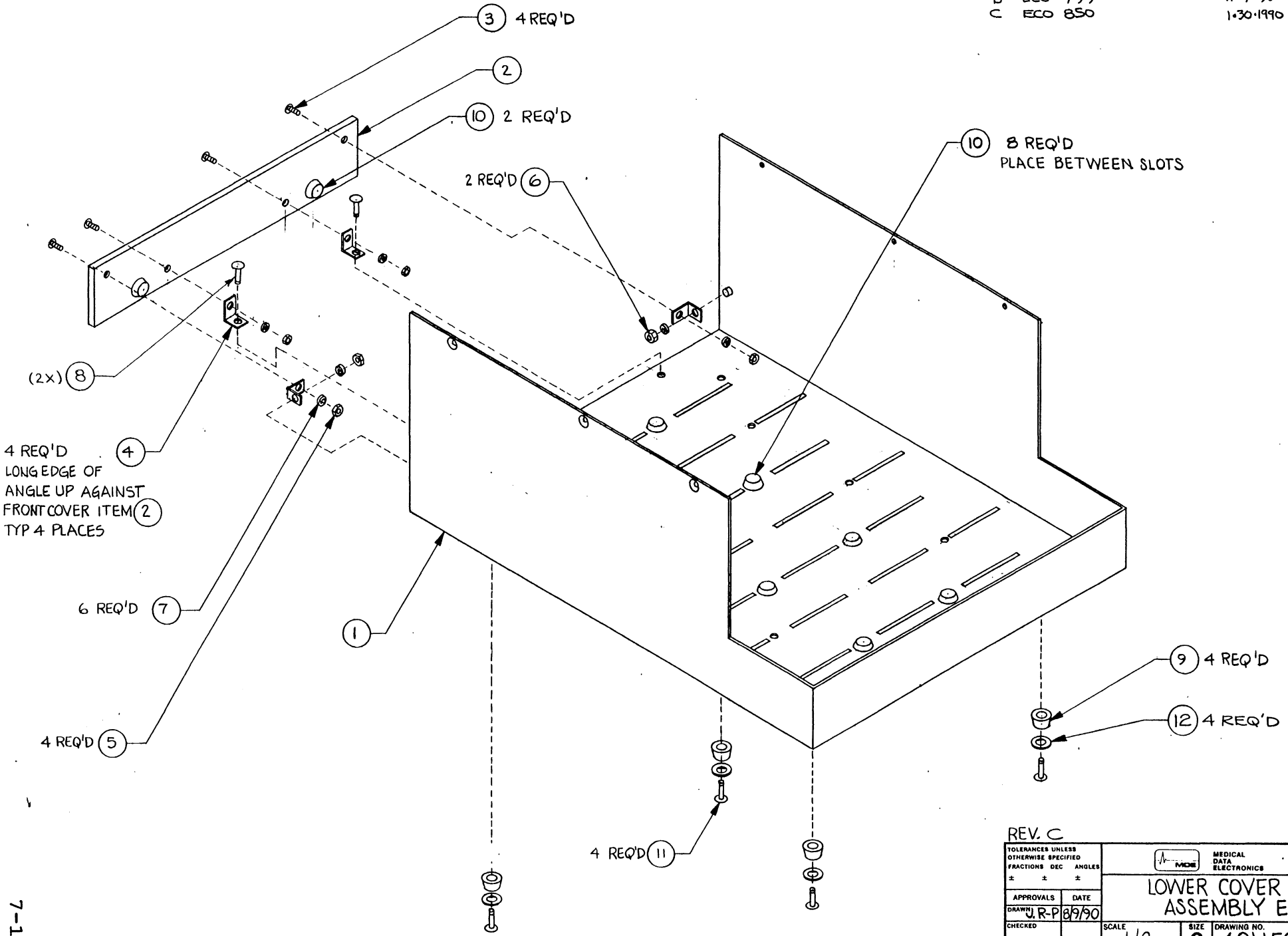
© SHOP GRAPHICS, INC

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ECO 689		
B	ECO 798	11-7-90	



TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		MEDICAL DATA ELECTRONICS	
APPROVALS	DATE	REAR PANEL ASSY E4	
DRAWN			
CHECKED		SCALE NONE	SIZE D DRAWING NO. 401158-0000
		DO NOT SCALE DRAWING	SHEET 1 OF 1

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE		
B	ECO 799	11-7-90	
C	ECO 850	1·30·1990	



REV. C

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		MEDICAL DATA ELECTRONICS
APPROVALS	DATE	LOWER COVER ASSEMBLY E4
DRAWN J.R-P	8/9/90	
CHECKED		SCALE 1/2 · SIZE C · DRAWING NO. 401159
		DO NOT SCALE DRAWING · SHEET 1 OF 1

7-10

BISHOP GRAPHICS, INC. REORDER NO. 20622

Assembly	Description	Group	PFC	Commodity	Class	Planner	Buyer	Drawing	Rev	LT
500116	CHASSIS ASSY, E4 REV. D (E934)				F				D	33

Shrinkage Factor: 0.000

ITEM	LEVEL	SEQ.	DESCRIPTION	REV	CL	LT	QUANTITY	U/M	REFERENCE	MLT	BEGIN	END
401159-0000	*1	1	LOWER COVER ASSY E4 REV. C (E850)	C	A	5	1.000	EA	1 - DO NOT ISSUE	Yes		
401156-0000	*1	2	BEZEL ASSY E4 REV. A		A	5	1.000	EA	2 - DO NOT ISSUE	Yes		
401158-0000	*1	3	REAR PANEL ASSY E4 REV. B (E798)	B	A	5	1.000	EA	3 - DO NOT ISSUE	Yes		
401138-0000	*1	5	PCBA, POWER SUPPLY E4 REV . A		A	5	1.000	EA	5 - DO NOT ISSUE	Yes		
401140-0000	*1	6	PCBA, Z-AXIS, E4 REV. C	C	A	5	1.000	EA	6	Yes		
401154-0000	*1	7	CABLE ASSY, Z-AXIS E4 REV . A		A	5	1.000	EA	7	Yes		
401153-0000	*1	8	HI VOLTAGE POWER SUPPLY A SSY, E4 REV. A		R	22	1.000	EA	8	Yes		
401149-0000	*1	9	CABLE ASSEMBLY, POWER SWI TCH E4 REV. A		A	5	1.000	EA	9	Yes		
401223-0000	*1	10	YOKE, CPU E4 REV. A		R	33	1.000	EA	10	Yes		
401148-0000	*1	11	SPEAKER ASSY, E4 REV. A		A	5	1.000	EA	11	Yes		
401542-0000	*1	12	VHF/UHF ACTIVE SPLITTER A SSY E4 REV. A (E930)	A	A	5	1.000	EA	12 - DO NOT ISSUE	Yes		
401112-0000	*1	13	BRACKET, CRT RIGHT E4 REV . A (E689)		R	33	1.000	EA	13	Yes		
401113-0000	*1	14	SUPPORT BRACKET, CRT E4 R EV. A (E689)		R	33	1.000	EA	14	Yes		
401114-0000	*1	15	MOUNTING BAR E4 REV. A		R	5	2.000	EA	15	Yes		
401118-0000	*1	16	FAB., UPPER HOUSING E4 RE V. B	B	A	5	1.000	EA	16	Yes		
401123-0000	*1	17	PROCESSOR MTG BRKT E4 REV . A		R	33	1.000	EA	17	Yes		
401124-0000	*1	18	MTG PLATE H.V.P.S. E4 REV . A (E689)		R	33	1.000	EA	18	Yes		
401131-0000	*1	19	SCREW, HOLD DOWN E4 REV. A		R	33	1.000	EA	19	Yes		
360500-0071A	*1	20	SPCR, #6 x 2 1/4"LG x 1/4 "O.D.,AL		R	33	1.000	EA	20 - DO NOT ISSUE	Yes		
360500-0072A	*1	21	SPCR, #6 x 1 1/4"LG x 1/4 "O.D.,AL		R	33	3.000	EA	21 - DO NOT ISSUE	Yes		
358100-0078A	*1	22	SCR, 8-32 x 3/8 SKTHD CAP , BLK		R	22	2.000	EA	22 - DO NOT ISSUE	Yes		
358100-0076A	*1	23	SCR, 4-40 x 5/8 SKTHD CAP SCR, BLK		R	33	9.000	EA	23 - DO NOT ISSUE	Yes		
401143-0000	*1	24	FAB PAINT SCR 6-32x1/4PH FLTHD (FM 358100-30A)-E4	A	A	33	12.000	EA	24 - DO NOT ISSUE	Yes		
358100-0080A	*1	25	SCR, 6-32 x 1 1/2 PH.PNHD PLTD		R	22	2.000	EA	25 - DO NOT ISSUE	Yes		

Assembly	Description	Group	PFC	Commodity Class	Planner Buyer	Drawing	Rev	LT
500116	CHASSIS ASSY, E4 REV. D (E934)			F			D	33

Shrinkage Factor: 0.000

ITEM	LEVEL	SEQ.	DESCRIPTION	REV	CL	LT	QUANTITY	U/M	REFERENCE	MLT	BEGIN	END
358100-0031A	*1	26	SCR, 4-40 X 3/8,BUTTON HD ,BLK OXIDE		R	11	4.000	EA	26 - DO NOT ISSUE	Yes		
358100-0036A	*1	27	SCR, 4-40 X 1/4,PH PNHD,C AD2 OR ANY		R	11	2.000	EA	27 - DO NOT ISSUE	Yes		
358100-0083A	*1	28	SCR, 4-40 x 1/2 PH FLTHD 82 DEG. CAD PLT		R	22	2.000	EA	28 - DO NOT ISSUE	Yes		
358100-0084A	*1	29	SCR, 6-32 x 5/16 PH PNHD (ANY PLATE)		R	22	10.000	EA	29 - DO NOT ISSUE	Yes		
358100-0055A	*1	30	SCR, 8-32 X 5/16,PH PNHD		R	11	4.000	EA	30 - DO NOT ISSUE	Yes		
358100-0011A	*1	31	SCR, 6-32 X 3/8,PH PNHD,C AD1 OR 2		R	11	6.000	EA	31 - DO NOT ISSUE	Yes		
358200-0009A	*1	32	WSHR, #4 SPLIT LOCK		R	11	2.000	EA	32 - DO NOT ISSUE	Yes		
358200-0010A	*1	33	WSHR, #6 SPLT LCK		R	11	16.000	EA	33 - DO NOT ISSUE	Yes		
358200-0011A	*1	34	WSHR, #8 SPLIT LOCK		R	11	4.000	EA	34 - DO NOT ISSUE	Yes		
360500-0023A	*1	35	NUT, #6 HEX,LRG PTRN		R	11	5.000	EA	35 - DO NOT ISSUE	Yes		
400712-0000	*1	36	FAB, FISH PAPER 23.26SQ"/ PC.(4.125" X 5.125")REV B		A	0	1.000	EA	36	Yes		
362000-0017A	*1	37	CRT DISPLAY E4		R	33	1.000	EA	37	Yes		
358200-0021A	*1	38	WSHR, #8 FLT STEEL,ANY PL ATING		R	11	4.000	EA	38 - DO NOT ISSUE	Yes		
358100-0091A	*1	39	SCR, 6-32 x 5/16 PHFLTHD PLTD 100 DEG.		R	11	12.000	EA	39 - DO NOT ISSUE	Yes		
358200-0006A	*1	40	WSHR, #6 FLT STL CAD 1		R	11	2.000	EA	40 - DO NOT ISSUE	Yes		
385000-0000A	*1	41	TY-WRAPS, 3IN LENGTH (1000/BAG)		R	11	14.000	EA	41 - DO NOT ISSUE	Yes		
358200-0018A	*1	42	WSHR, #6 INT TOOTH STEEL		R	11	8.000	EA	42 - DO NOT ISSUE	Yes		
401111-0000	*1	46	PANEL, CPU E4 REV. B	B	R	33	1.000	EA	45	Yes		
401348-0000	*1	49	FAB - FISH PAPER PWR SUPP LY E4		A	5	1.000	EA	47	Yes		
385000-0017A	*1	50	CABLE TIE MOUNT, ADHESIVE BACKED		R	11	1.000	EA	48 - DO NOT ISSUE	Yes		
401347-0000	*1	51	LBL, SERIAL NUMBER E3/E4		R	22	1.000	EA	49 - DO NOT ISSUE	Yes		
401134-0000	*1	52	PCBA, E4 CPU REV. D (E897)	D	A	5	1.000	EA	4 - DO NOT ISSUE	Yes		
400404-0000	*1	53	LABEL, "UL LISTED MEDICAL EQUIP." 26T1 -E3/E4		R	30	1.000	EA	50	Yes		

Cumulative Lead Time for 500116 = 66

ANTENNA SYSTEM DESIGN

CHAPTER 8

SECTION 1

ANTENNA SYSTEM DESIGN

ANTENNA LOCATIONS

The first step in designing an antenna system is to determine the location(s) of antennas necessary for reception of adequate RF telemetry signals under the worst possible conditions. A scale plan view of the desired area(s) to be covered should be drawn and locations selected based on the physical characteristics of construction for the area involved. Antennas should be located as high as possible (ceiling level) to best eliminate the effects of people and objects in the covered areas.

The second step involves determining the materials used for partitions and walls. This information can usually be obtained from hospital building maintenance department, and original detailed construction plans are frequently available. Table I shows estimated design distances that may be used when the construction materials are known.

In addition to partitions and wall materials, the ceiling construction should be investigated. Determine the locations of any large metal areas such as heating and cooling ducts, metal lath beneath plaster, foil backed insulation, or wire reinforced ceiling panels. If it is necessary to mount antennas below these metal objects, space the antenna by at least 8 inches from ceiling surfaces. The 8 inch spacing is a copromise, and therefore, there is some degradation of antenna performance. When this problem exists, the coverage areas shown in Table I should be reduced to 75%.

In preparing a scale layout of the areas to be covered, locate the antennas by using the recommended design distances shown in Table I. Allow the antenna coverage to overlap, creating areas to equal the antenna design radius of at least one receiving antenna. An example of a scale plan layout is shown in Fiqure 1-2.

In very simple systems at least two antennas should be used. This reduces the possibility of a drop-out from occurring if blockage or reflection by a piece of equipment causes loss of signal to a single antenna.

From the detailed construction plans, determine any special construction details that may shield the antenna from the patient transmitter. These may include any of the following:

- Steel automatic fire doors
- Elevator shafts
- X-ray rooms (shielded)
- Large installations of metal racks for food
- service, laundries, etc.
- Air conditioning or heating ducts over approximately 20" wide
- Foil-covered insulation

Assume when developing the scale layout that these details will block all telemetry signals. Where such cases of signal interference are known, it is recommended that the maximum distances from these objects to an antenna be reduced to 50% of the distances given by Table I. Figure 1.2 is an example of a floor plan where several such features are represented. Schematics and sample calculations are shown in figures 1.3 and 1.4 respectively.

CABLE ROUTING

After the estimated location(s) of antennas has been determined, possible routing of interconnecting wiring should be laid out on the scale drawing to determine cable length required. Cable lengths should be kept as short as possible to minimize losses. In order to achieve balanced gain from each antenna to the first associated multiplexer, the cables from each antenna should be approximately the same length; i.e., situate the multiplexer equidistant from its associated antennas. The losses can usually be equalized by physical location of the multiplexer or selection of appropriate cable type. Note in Fiqure 1-3 that all antennas to the first multiplexers are at equal distances.

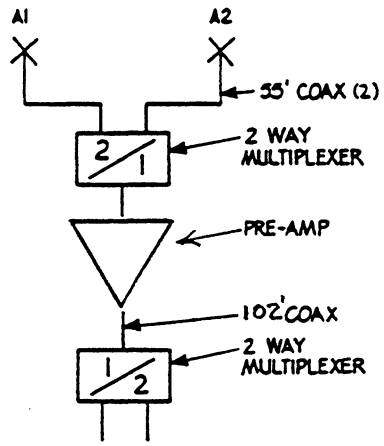
Caution: Many inexpensive RG59U cables are available. Some have been found to have high losses or provide a poor impedance match. It is recommended that only quality cables be used from a reliable supplier.

Avoid routing cables in areas with potential sources of electrical noise such as diathermy, data processing equipment, radio or CATV equipment, heavy electric motors, or elevators wiring and switches. If it is necessary to run lines near others that could be carrying interfering electrical signals, they should be separated as far as possible, and if they intersect, they should be routed at right angles, and through 1/2" rigid conduit grounded at both ends.

SYSTEM LOSS/GAIN CALCULATIONS

A system schematic should be drawn to calculate total losses and determine where amplifiers are required. The goal should be to design a system with zero losses from the antenna to the receiver . Table II shows standard electrical symbols and the losses or gains associated with the elements required for installation. These losses are based on midband frequencies in TV channel 9 or 10. Slight variations will exist for systems using TV channels 7 or 13. However, these variations amount to less than 5% and can therfore be disregarded.

Systems losses are calculated by summing the losses of individual components. A simplified diagram of a system schematic is shown in the adjacent chart. As shown, the dB loss/gain for each component, as obtained from Table II, are totalled to determine the overall loss/gain of 0 dB.



COMPONENT	COMPONENT LOSS	CUMULATIVE GAIN/LOSS
A1 OR A2 ANTENNA	0	0
55' FOAM COAX RG59/μ	-2.2	-2.2
2 WAY MULTIPLEXER	-3.8	-6.0
PRE-AMP	+14.0	+8.0
10Z' FOAM COAX RG59/μ	-4.2	+3.8
2 WAY MULTIPLEXER	-3.8	0

FIQURE 1-1 Simplified System Diagram

Fiqure 1-2 is an example of a scale plan layout for a more complex system. Fiqure 1-3 shows the corresponding schematic. Sample calculations are shown in Fiqure 1-4.

The sections specified as "without preamplication" are preliminary calculations to determine the total path losses of all elements, and they thereby enable determination of the best locations for the required preamplifiers. It is important to provide amplification in any system before the losses become large enough to increase the inherent noise generated by preamplifiers.

PREAMPLIFIER NOISE

Each preamplifier added to the system contributes additional low level noise to the signals being transmitted, the amount of which is indicated in preamplifier specifications as "Noise Figure." This noise has the effect of decreasing the effective range of antennas for useable clean RF signals. Calculations for evaluating the effects of Noise Figure and antenna effective range are beyond the scope of these instructions. The rules outlined below are critical in achieving the effective ranges outlined in Table I.

1. No total individual cumulative circuit path loss can be greater than 40 dB.
2. No more than 2 preamplifiers limited to 20 dB maximum gain should be included in each circuit path.
3. First preamplifier gain must be added before the losses from any antenna are greater than -10 dB.
4. A second preamplifier stage should be added when the cumulative gain/loss is greater than 0 dB.

Table I
Antenna Spacing VS Wall Construction

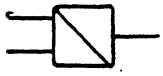
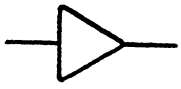
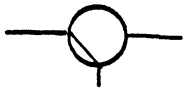
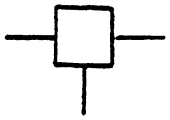
Wall Construction Type	Coverage Area Omni-directional Antenna
I. 1. Wood studs & Sheet-rock 2. Wood studs & plaster on gyspsum board 3. Vertical metal studs greater than 4 feet centers 4. Concrete or block with plaster	60 ft. radius
II. 1. Metal studs 24" O.C. 2. Metal studs with plaster on gypsum board. 3. Reinforced concrete 36" O.C. minimum reinforcing bars	50 ft. radius
III. 1. Foil backed sheet-rock 2. Alum. foil insulation 3. Plaster on metal lath 4. Steel paneling	Line of sight to antenna 50 ft. radius max.

NOTE: 1. Reduce distance shown to 75% when there is metal in the ceiling such as metal lath or air conditioning ducts.

2. Distance shown are based on receiver sensitivities of 1 uV or better.

Table II

Component Loss/Gain Characteristics

SCHEMATIC SYMBOL	ELEMENT	LOSS/GAIN	DC CURRENT @ 14 TO 20 VDC	MDE P/N
	Omni-directional			340000-0001 * TL1800
	Omni-directional Antenna 450-470 Mhz			340000-0010 * TL4750
	Two-way multiplexer	-3.8 dB		340000-0002
	Four-way Multiplexer	-7.5 dB		340000-0003
	RG/59 Cable Solid Polyethelene	-4.9 dB/100'		Belden #8241
	RG/59 Cable Foam Polyethylene	-4.1 dB/100'		Belden #8221
	Terminator	0 dB		340000-0013
	Preamplifiers: 174-216 MHz	+14 dB	55 Ma.	340000-0005 * TA214
	174-216 MHz	+26 dB	85 Ma.	340000-0004 * TA213
	450-470 MHz	+17 dB	55 Ma.	340000-0009 * TA1483
	Directional Coupler insertion loss	-7dB -1dB		340000-0016
	Directional Coupler insertion loss	-12dB -.6dB		340000-0017
	Directional coupler insertion loss	-17dB -.5dB		340000-0018
	Power Supply	-20 VDC	500 Ma.	340000-0008 * PS2000

* Winegard Part Number

SCALE FLOOR PLAN

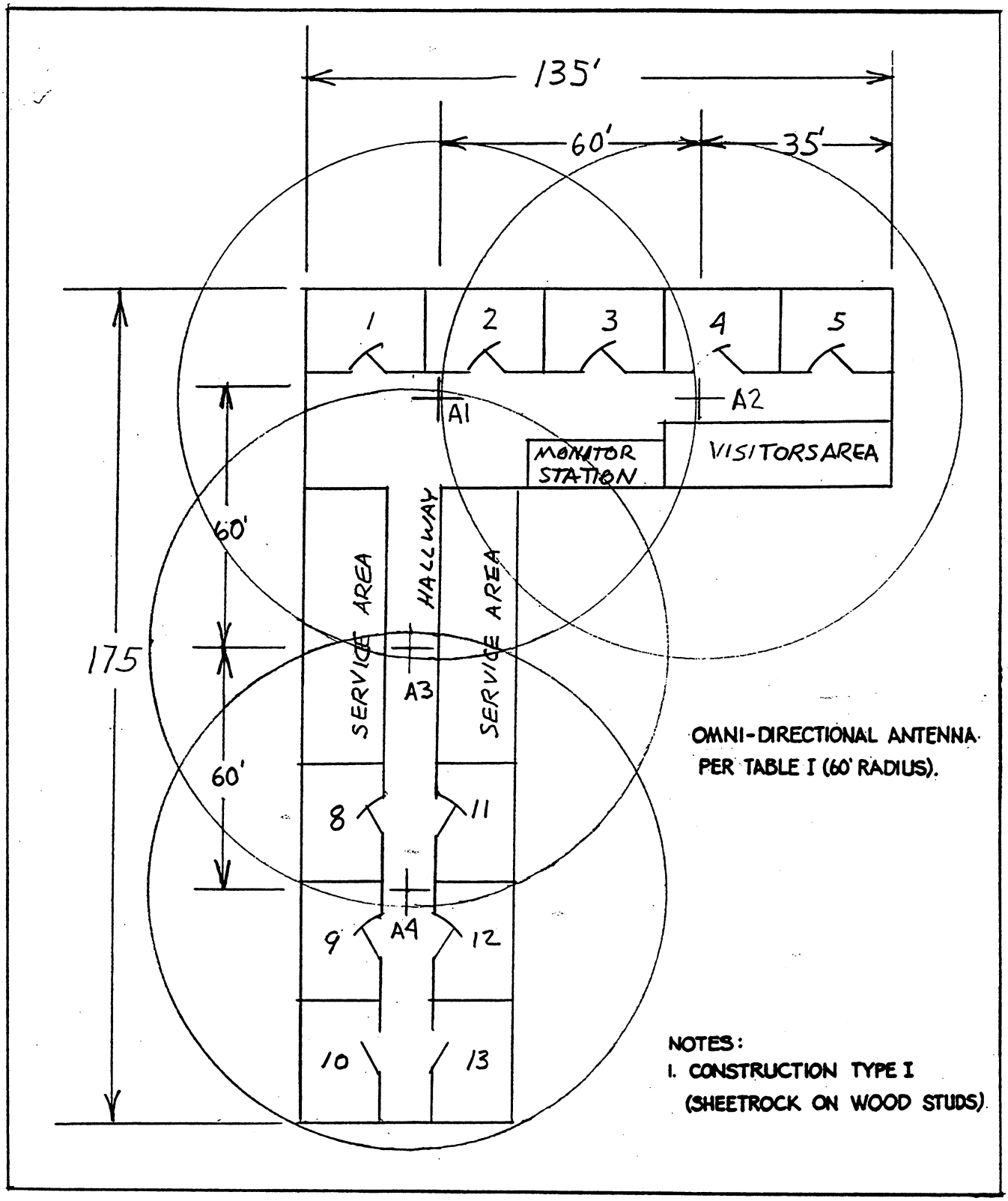


Fig. 1-2

SCHEMATIC

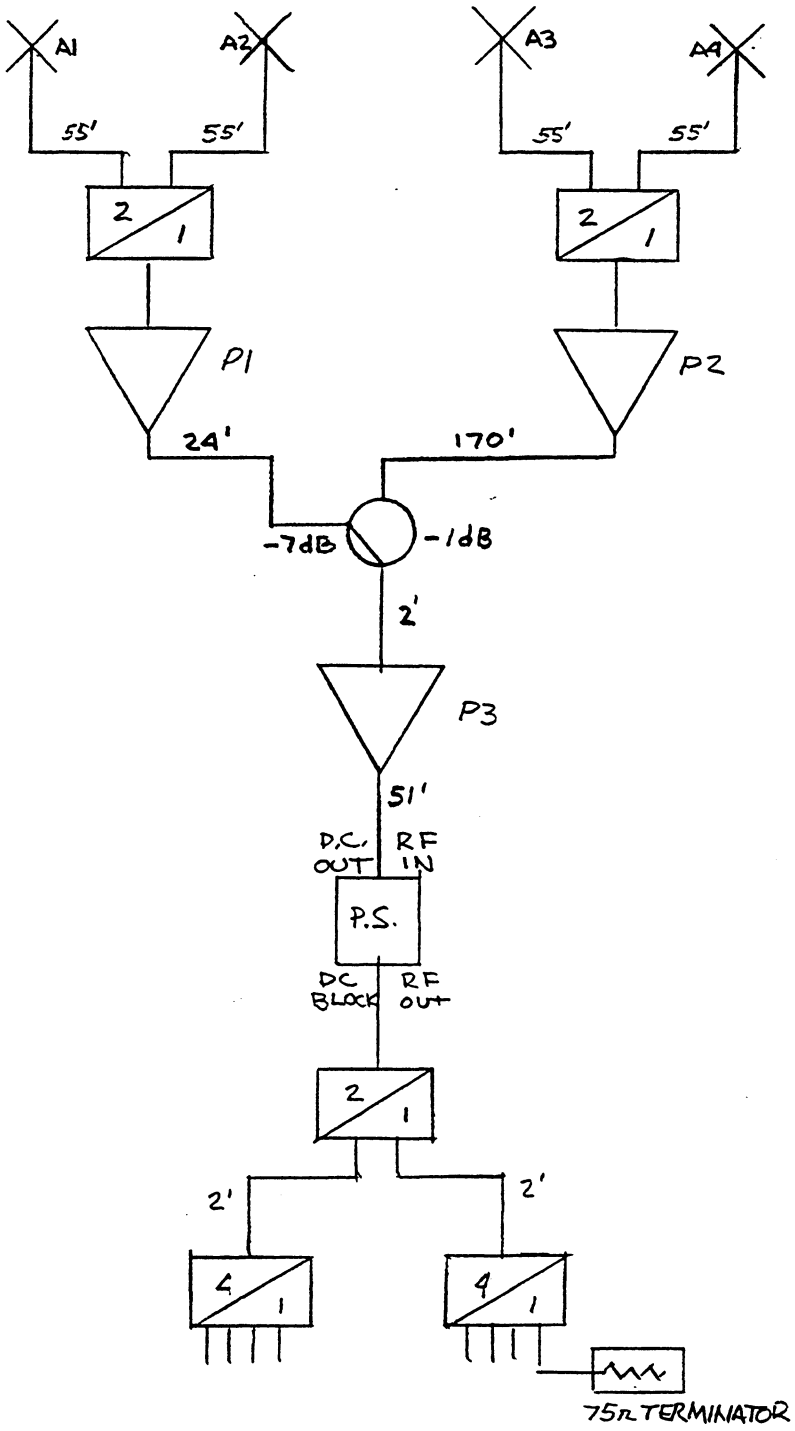


Fig. 1-3

SAMPLE CALCULATIONS

ANTENNA PATH – FROM A1 OR A2 TO MONITOR
WITHOUT PREAMPLIFICATION WITH PREAMPLIFICATION

COMPONENT	COMPONENT LOSS	CUMULATIVE GAIN/LOSS
A1 OR A2 BIDIR. ANTENNA	0	0
55' RG 59/μ FOAM CABLE	-2.2	-2.2
TWO WAY MULTPLX	-3.8	-6.0
24' RG 59/μ FOAM CABLE	-1.0	-7.0
DIRECT. COUPLR.	-7.0	-14.0
51' RG 59/μ FOAM CABLE	-2.1	-16.1
PWR SUPPLY COUPLER	-0.5	-16.6
TWO WAY MULTPLX	-3.8	-20.4
2' RG 59/μ FOAM CABLE	-0.1	-20.5
FOUR WAY MULTPLX	-7.5	-28.0
TOTAL		

COMPONENT	COMPONENT LOSS	CUMULATIVE GAIN/LOSS
A1 OR A2 BIDIR. ANTENNA	0	0
55' RG 59/μ FOAM CABLE	-2.2	-2.2
TWO WAY MULTPLX	-3.8	-6.0
PREAMPLIFIER - P1	+14.0	+8.0
24' RG59/μ FOAM CABLE	-1.0	+7.0
DIRECT. COUPLR.	-7.0	0
PREAMPLIFIER - P3	+14.0	+14.0
51' RG59/μ FOAM CABLE	-2.1	+11.9
PWR SUPPLY COUPLER	-0.5	+11.4
TWO WAY MULTPLX	-3.8	+7.6
2' RG59/μ FOAM CABLE	-0.1	+7.5
FOUR WAY MULTPLX	-7.5	0
TOTAL		0

ANTENNA PATH FROM A3 OR A4 TO MONITOR
WITHOUT PREAMPLIFICATION WITH PREAMPLIFICATION

COMPONENT	COMPONENT LOSS	CUMULATIVE GAIN/LOSS
A3 OR A4 ANTENNA	0	0
55' RG 59/μ FOAM CABLE	-2.2	-2.2
TWO WAY MULTPLX	-3.8	-6.0
170' RG 59/μ FOAM CABLE	-7.0	-13.0
DIRECT. COUPLR	-1.0	-14.0
RG 59/μ FOAM CABLE	-2.1	-16.1
PWR SUPPLY COUPLER	-0.5	-16.6
TWO WAY MULTPLX	-3.8	-20.4
2' RG 59/μ FOAM CABLE	-0.1	-20.5
FOUR WAY MULTPLX	-7.5	-28.0
TOTAL		

COMPONENT	COMPONENT LOSS	CUMULATIVE GAIN/LOSS
A3 OR A4 ANTENNA	0	0
55' RG 59/μ FOAM CABLE	-2.2	-2.2
TWO WAY MULTPLX	-3.8	-6.0
PREAMPLIFIER - P2	+14.0	+8.0
170' RG 59/μ FOAM CABLE	-7.0	+1.0
DIRECT. COUPLR.	-1.0	0
PREAMPLIFIER - P3	+14.0	+14.0
51' RG 59/μ FOAM CABLE	-2.1	+11.9
PWR SUPPLY COUPLER	-0.5	+11.4
TWO WAY MULTPLX	-3.8	+7.6
2' RG 59/μ FOAM CABLE	-0.1	+7.5
FOUR WAY MULTPLX	-7.5	0
TOTAL		0

Fig. 1-4

ANTENNA SYSTEM TESTS

TELEMETRY SYSTEM TESTS

System Tests should be conducted on all newly installed antenna systems to insure good electrical connections and balanced RF gain.

ELECTRICAL TESTS – STATIC

After design and installation of wiring, and prior to antenna system turn-on, a static test should be performed to insure good cable connections and grounding. Prior to applying antenna power, connect the power, connect the power coupler and multiplexers to the coaxial lines. Do not connect preamplfiers Couple all preamplifier input and output lines with RF connector. Place an ohm meter on the input to the power supply coupler (no power applied) between DC voltage input and ground. It should be an open circuit greater than 100k ohms. If this reading is low, it indicates a shorted connector or cable. Remove connections one at a time to isolate the faulty wiring.

After verifying the open substitute a test 75 ohm load at one antenna connnection. The DC resistance measured at the power supply coupler should be 75 ohms. Repeat for each of the antenna input leads in the system. This insures continuity to each of the antenna inputs.

RF CONDUCTED GAIN TEST

Connect a signal generator to one of the antenna inputs. Connect Rf Spectrum Analyzer to antenna system output. Generator should be set for 188 Mhz at -60 dBm. The gain from antenna input to antenna system output should be 0 dB ±3dB. This test should be repeated for each antenna input.

ANTENNA SYSTEM RANGE TEST

Connect an MDE telemetry monitor to the output of the antenna system. With the aid of an assistant who is hooked up to telemetry transmitter, walk through the area covered by the antenna system.

Verify that the the observed signal remains noise free or that only momentary short-term (2 sec. or less) noise bursts occur under the longest range conditions.

Marginal performance may be caused by:

1. Hidden metal objects such as air conditioning ducts or other metal conduits detuning an antenna.
2. Large metal objects deflecting the transmitted signal.
3. Improperly located antenna(s).

These conditions can usually be corrected by spacing the antenna(s) away from metal objects, mounting the antenna(s) on extenders, changing antenna location(s) by a few feet, or in more severe cases, by adding an antenna to cover the problem area. Note, however, that if an additional antenna(s) is added, it will be necessary to rebalance the system to maintain an antenna system gain of 0dB +3db.

Medical Data Electronics • 12720 Wentworth Street • Arleta, California 91331-4329
(800) 237-5243 • (818) 768-6411 • FAX (818) 768-0759

P/N 401389-0000

recycled paper